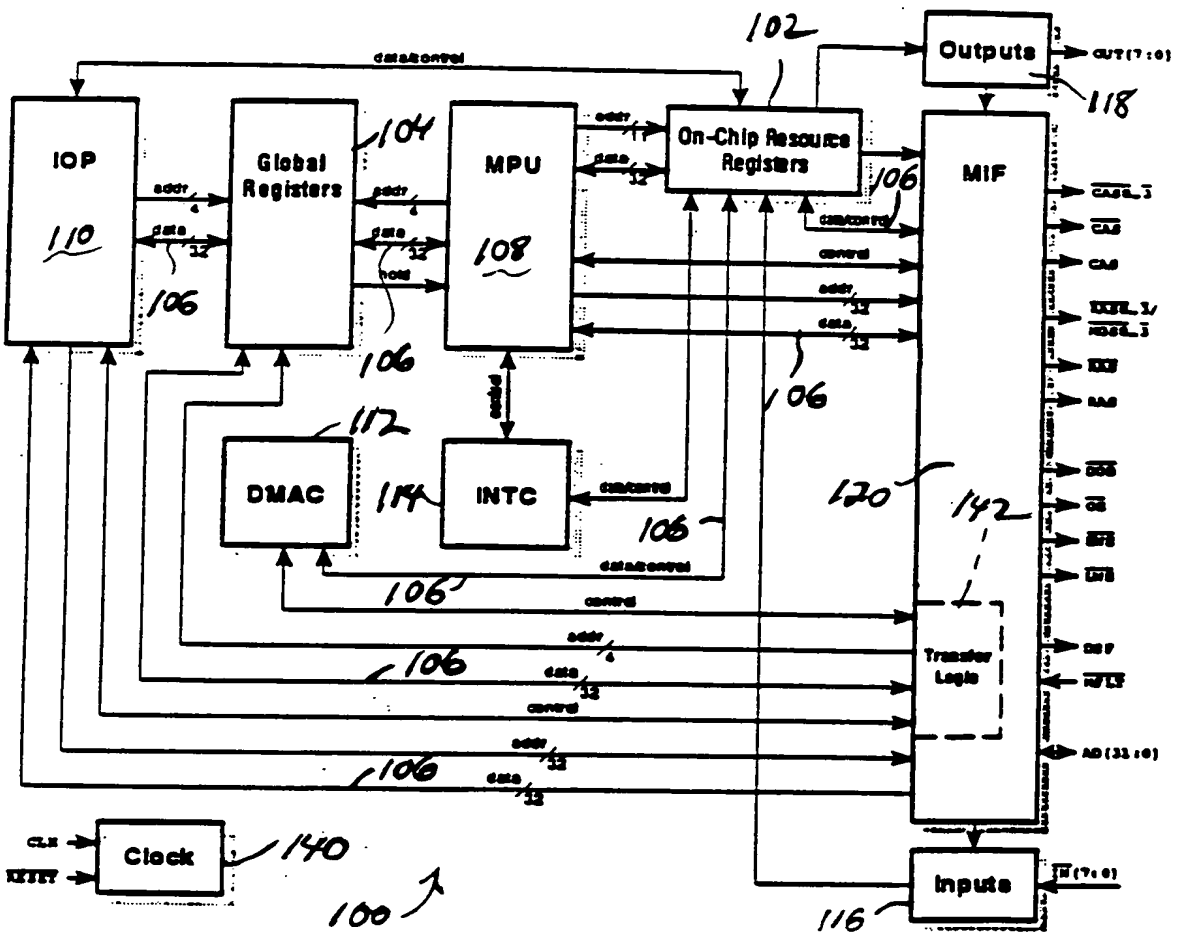

FIG. 1

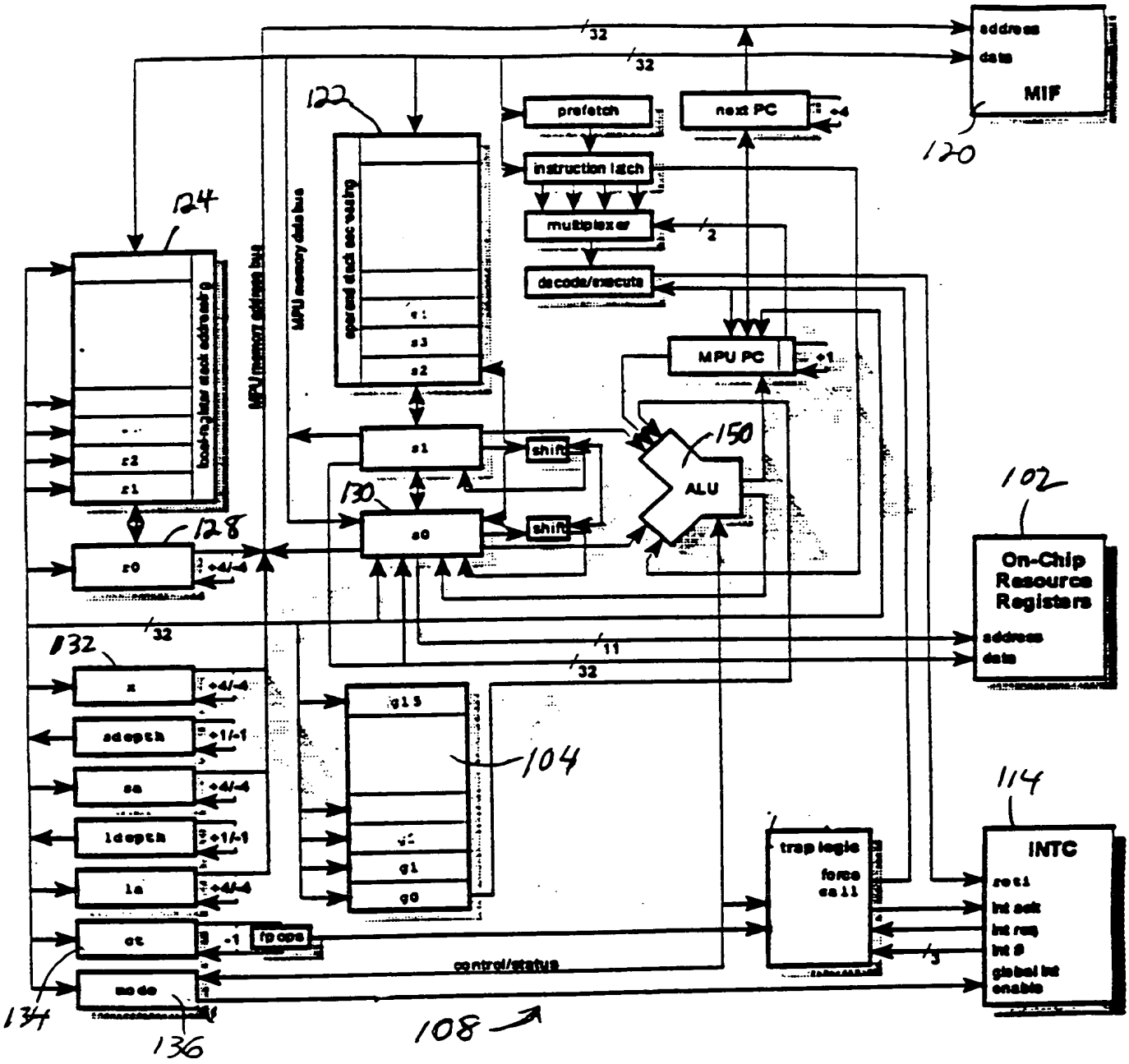
address
data
MIF
120
32
32
122
prefetch
next PC
+4
instruction latch
multiplexer
2
decode/execute
124
MPU PC
+1
150
ALU
shift
shift
130
128
102
On-Chip Resource Registers
address
data
11
32
132
104
114
INTC
trap logic
force call
control/status
108
134
136

FIG. 2

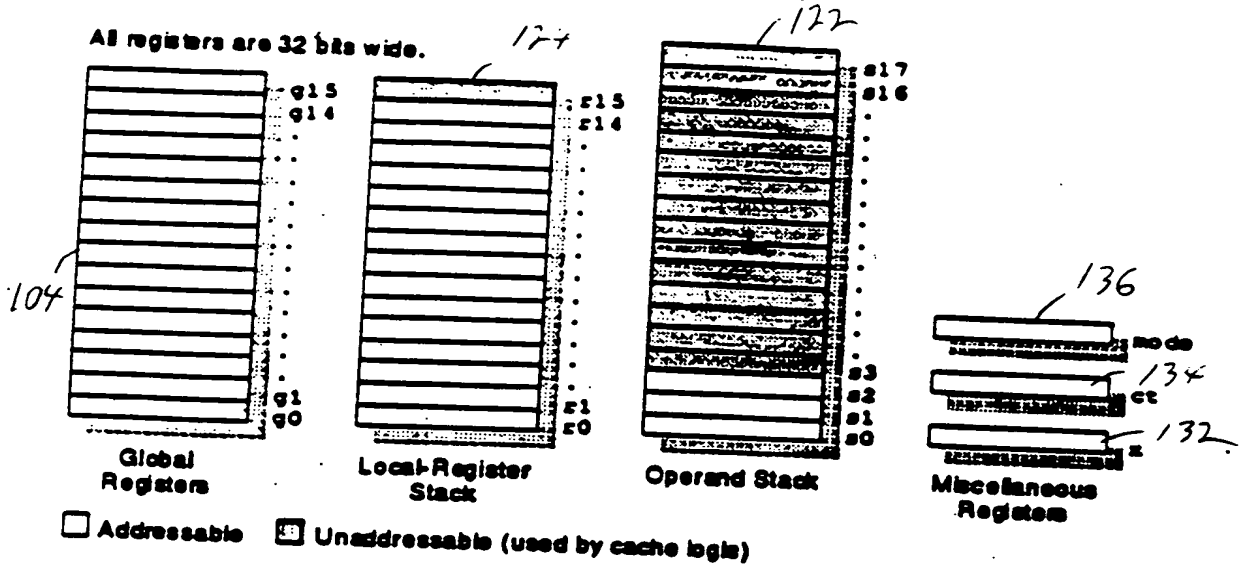

FIG. 3

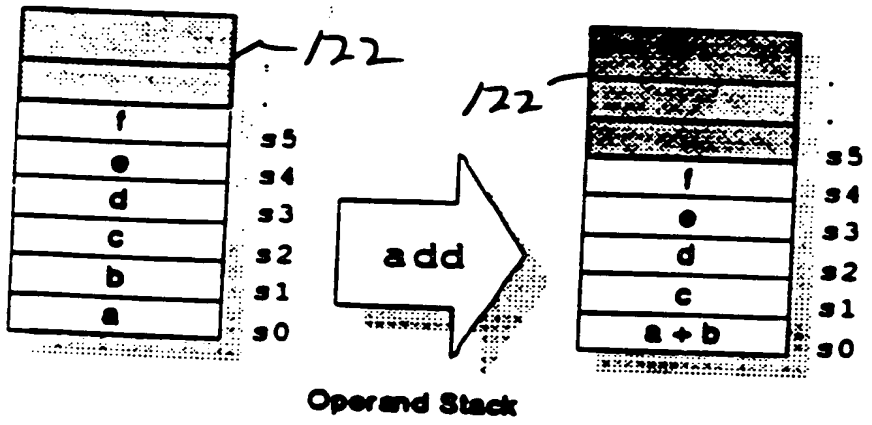

FIG. 3a

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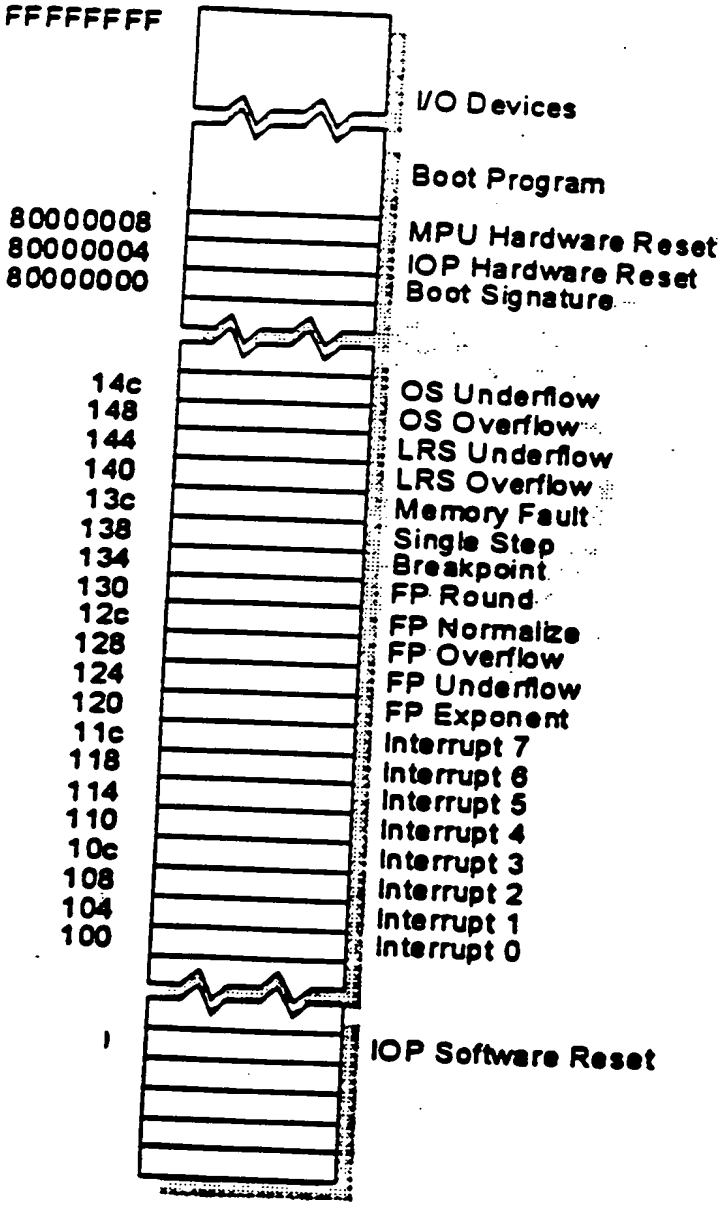

FIG. 4

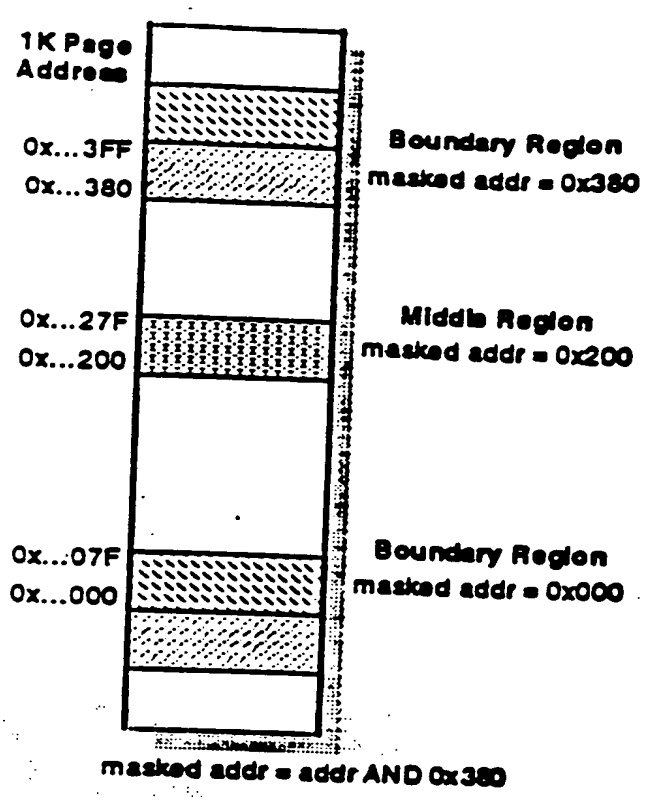
550
1K Page Address
0x...3FF
0x...380
Boundary Region
masked addr = 0x380
0x...27F
0x...200
Middle Region
masked addr = 0x200
0x...07F
0x...000
Boundary Region
masked addr = 0x000
masked addr = addr AND 0x380

FIG. 5

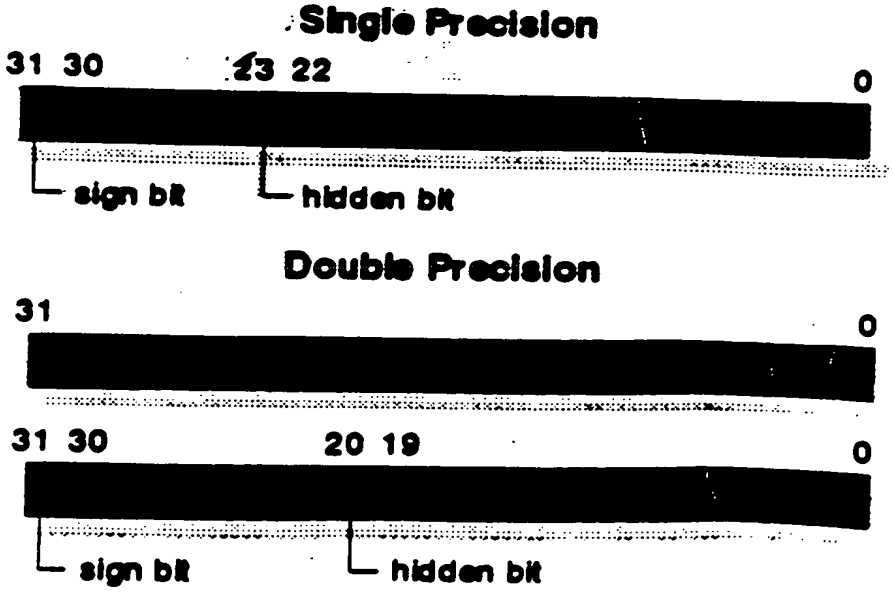
Single Precision
31 30
23 22
0
sign bit
hidden bit
Double Precision
31
0
31 30
20 19
0
sign bit
hidden bit

FIG. 6a

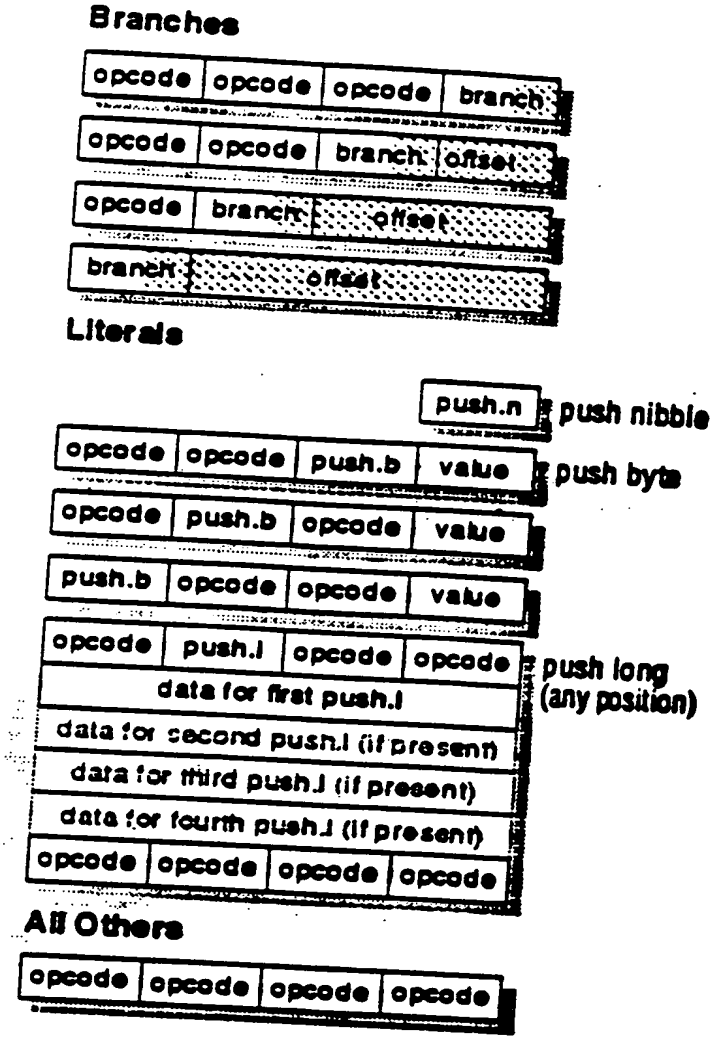

FIG. 6

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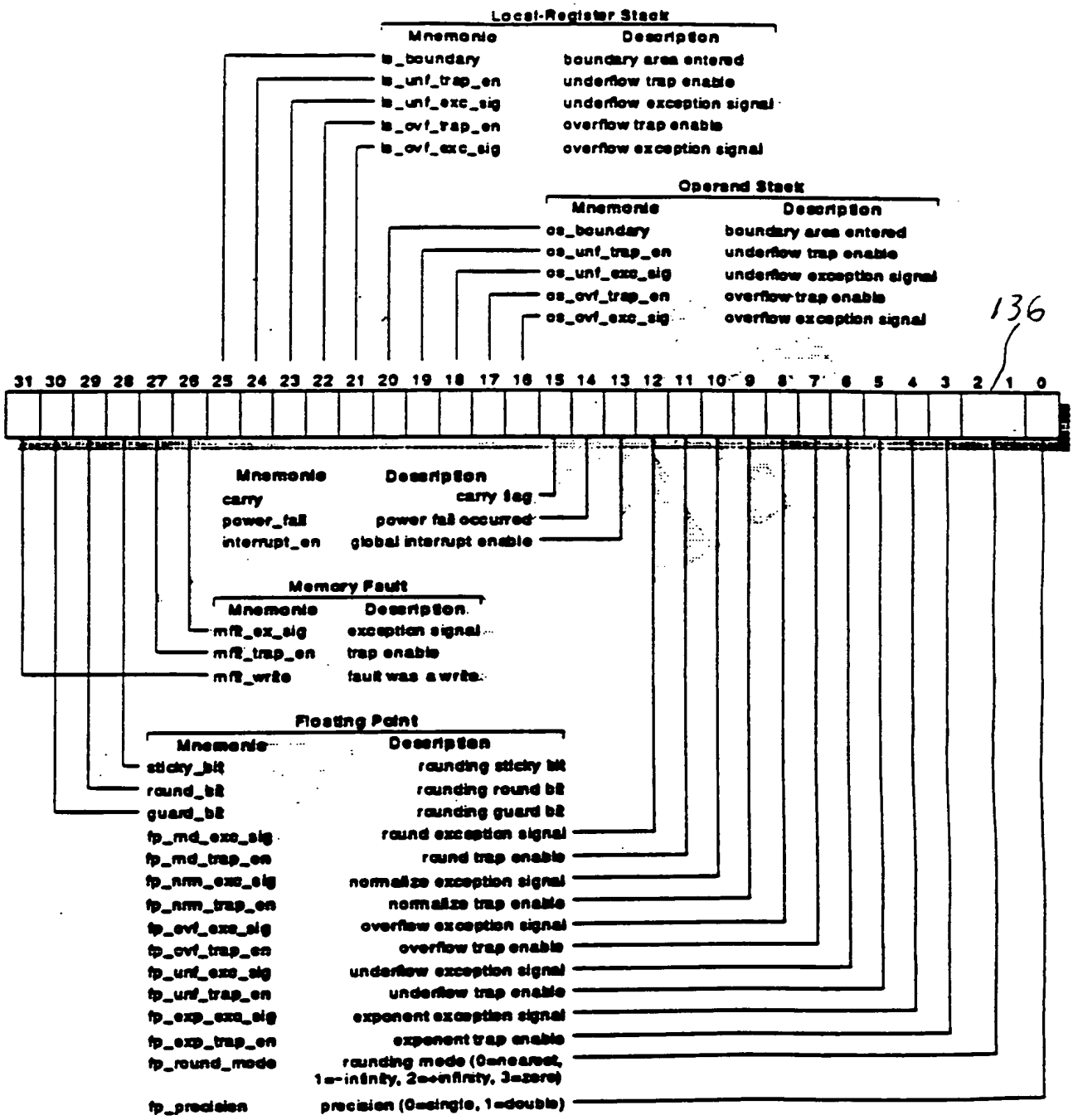

FIG. 7

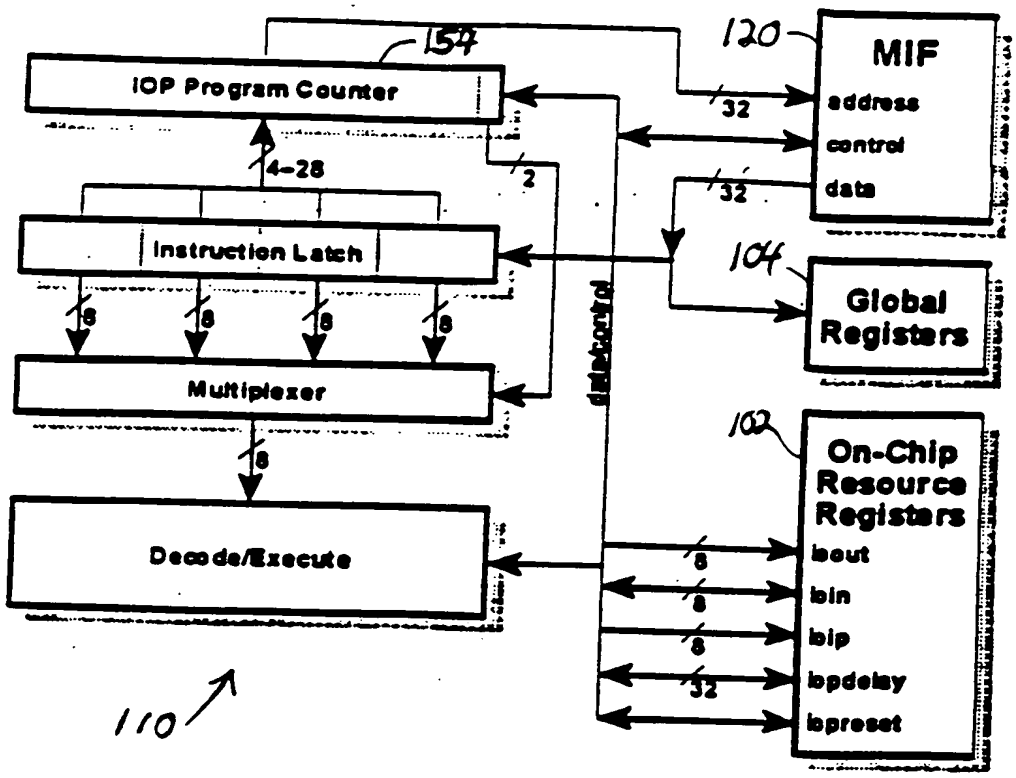

FIG. 8

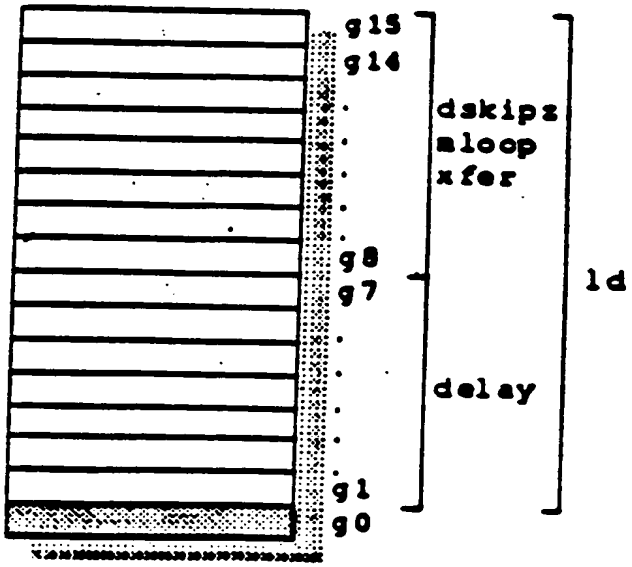

FIG. 9

Branches

opcode	opcode	opcode	branch
opcode	opcode	branch	offset
opcode	branch	offset	
branch	offset		

Literals

opcode	ld #,gn	opcode	opcode
data for first ld #,gn			
data for second ld #,gn (if present)			
data for third ld #,gn (if present)			
data for fourth ld #,gn (if present)			
opcode	opcode	opcode	opcode

load register (any position)

All Others

opcode	opcode	opcode	opcode

FIG. 10

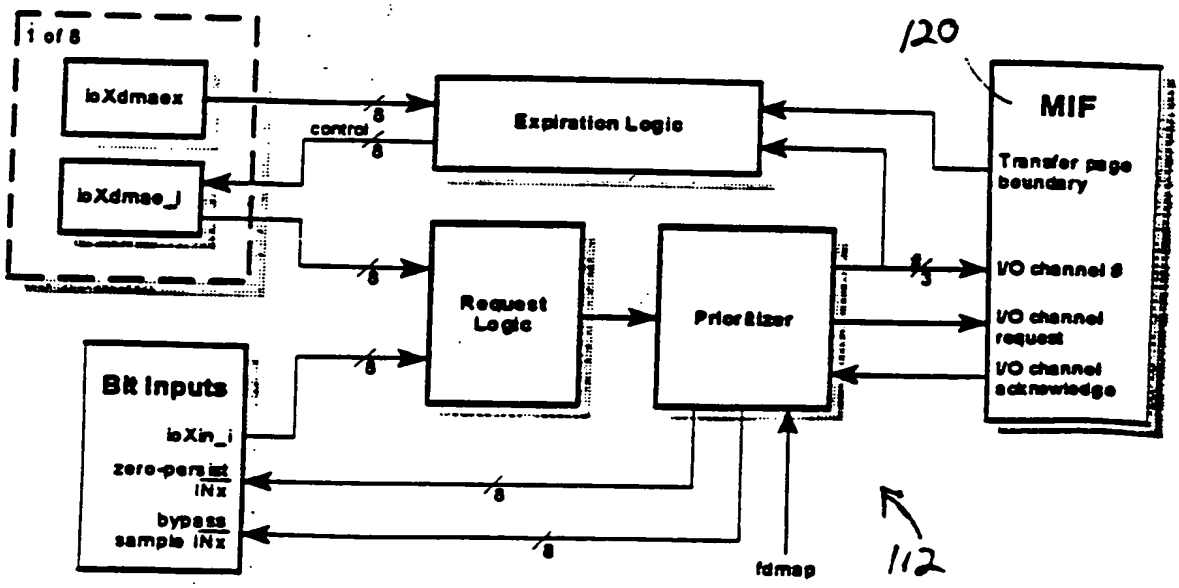

FIG. 11

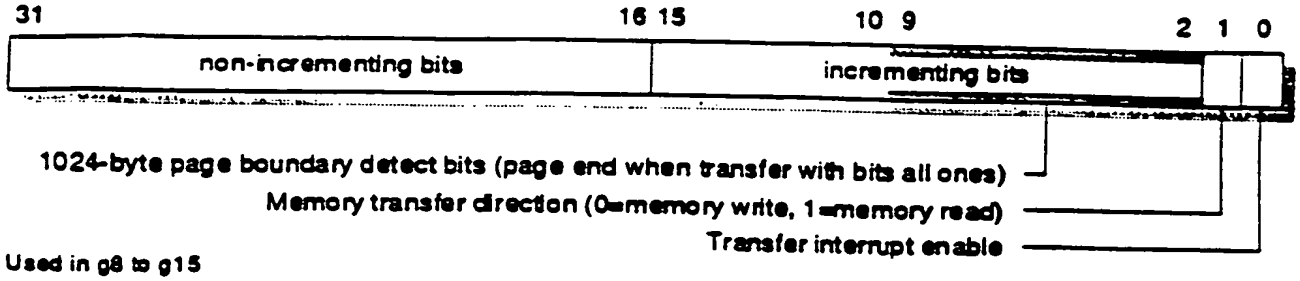
31
16 15
10 9
2 1 0
non-incrementing bits
incrementing bits
1024-byte page boundary detect bits (page end when transfer with bits all ones)
Memory transfer direction (0=memory write, 1=memory read)
Transfer interrupt enable
Used in g8 to g15

FIG. 12

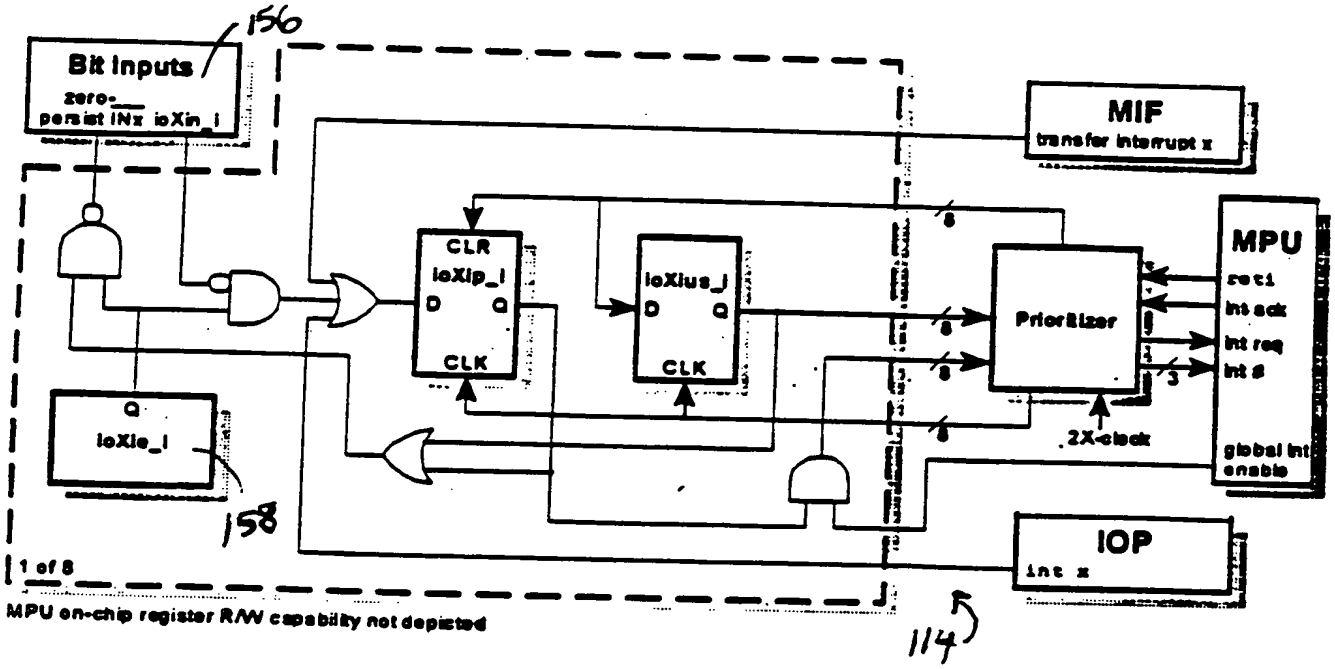
156
Bit Inputs
zero-
persist INx ioXin_i
MIF
transfer interrupt x
CLR
ioXip_i
D Q
CLK
ioXius_i
D Q
CLK
Prioritizer
MPU
ioXie_i
158
2X-clock
global int enable
IOP
int x
1 of 8
MPU on-chip register R/W capability not depicted
114

FIG. 13

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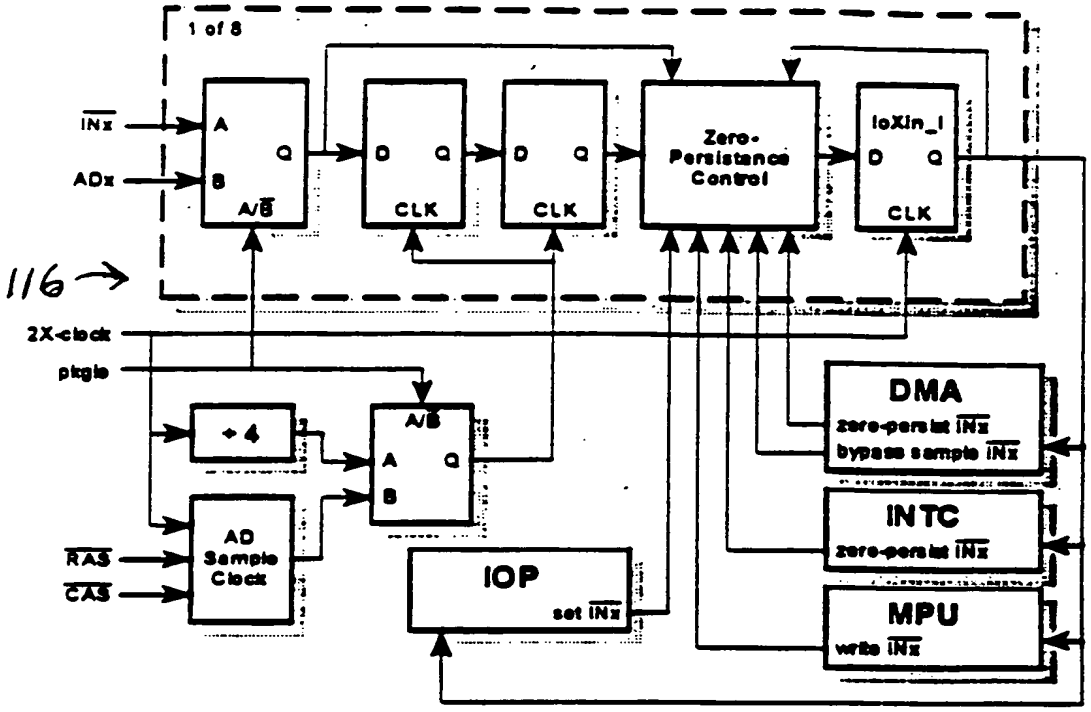


FIG. 14

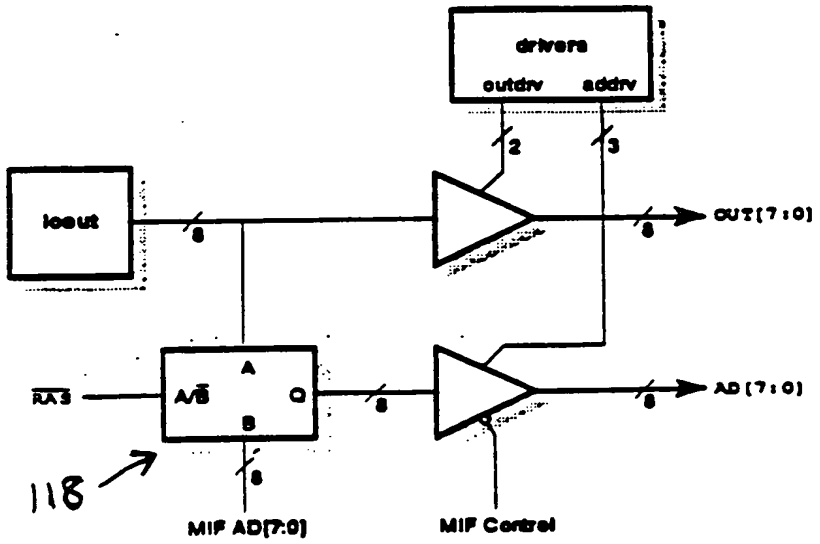
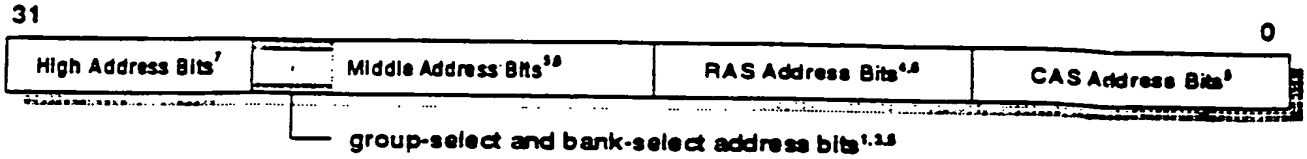
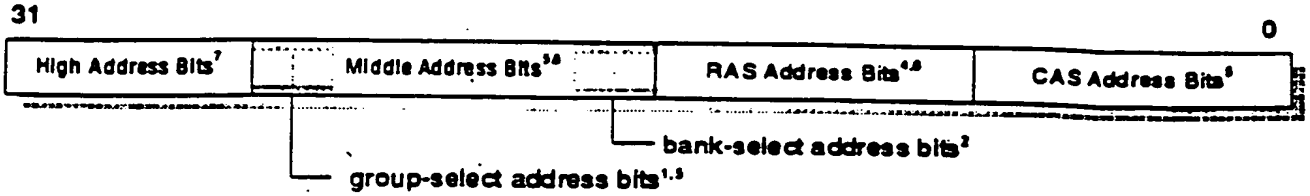


FIG. 15

SMB — Single Memory Bank per Memory Group Mode



MMB — Multiple Memory Bank per Memory Goup Mode



Notes

1. Located by bits in `msgsm`.
2. DRAM—2 bits immediately above the RAS address bits.
   SRAM—2 bits located by `mssbs` in `misc`.
3. SRAM and DRAM.
4. DRAM only, field is zero length in SRAM.
5. Excluded from RAS-cycle determination, except for A31 (see note 7).
6. Included in RAS-cycle determination.
7. Optionally included in RAS-cycle determination.
8. If `msgsm` is zero, see text.

FIG. 16

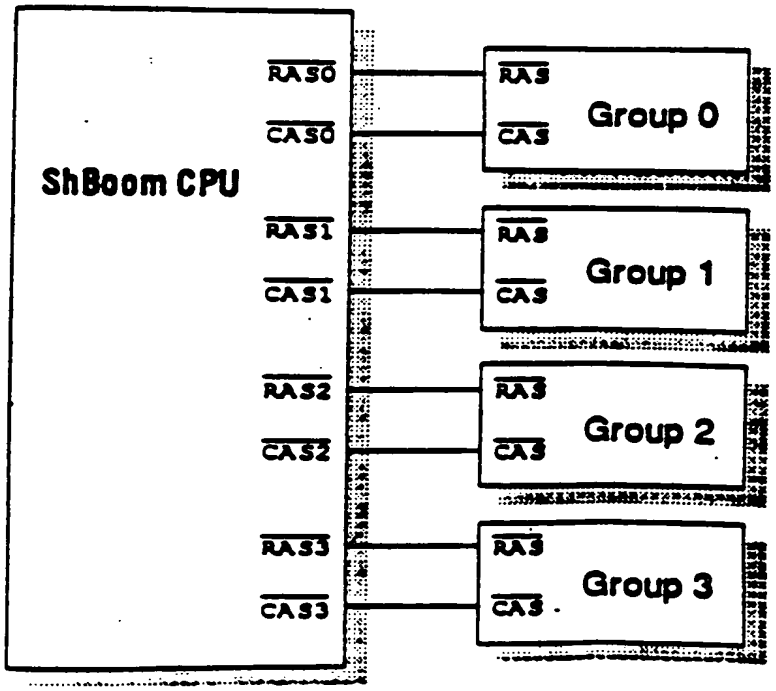


FIG. 17

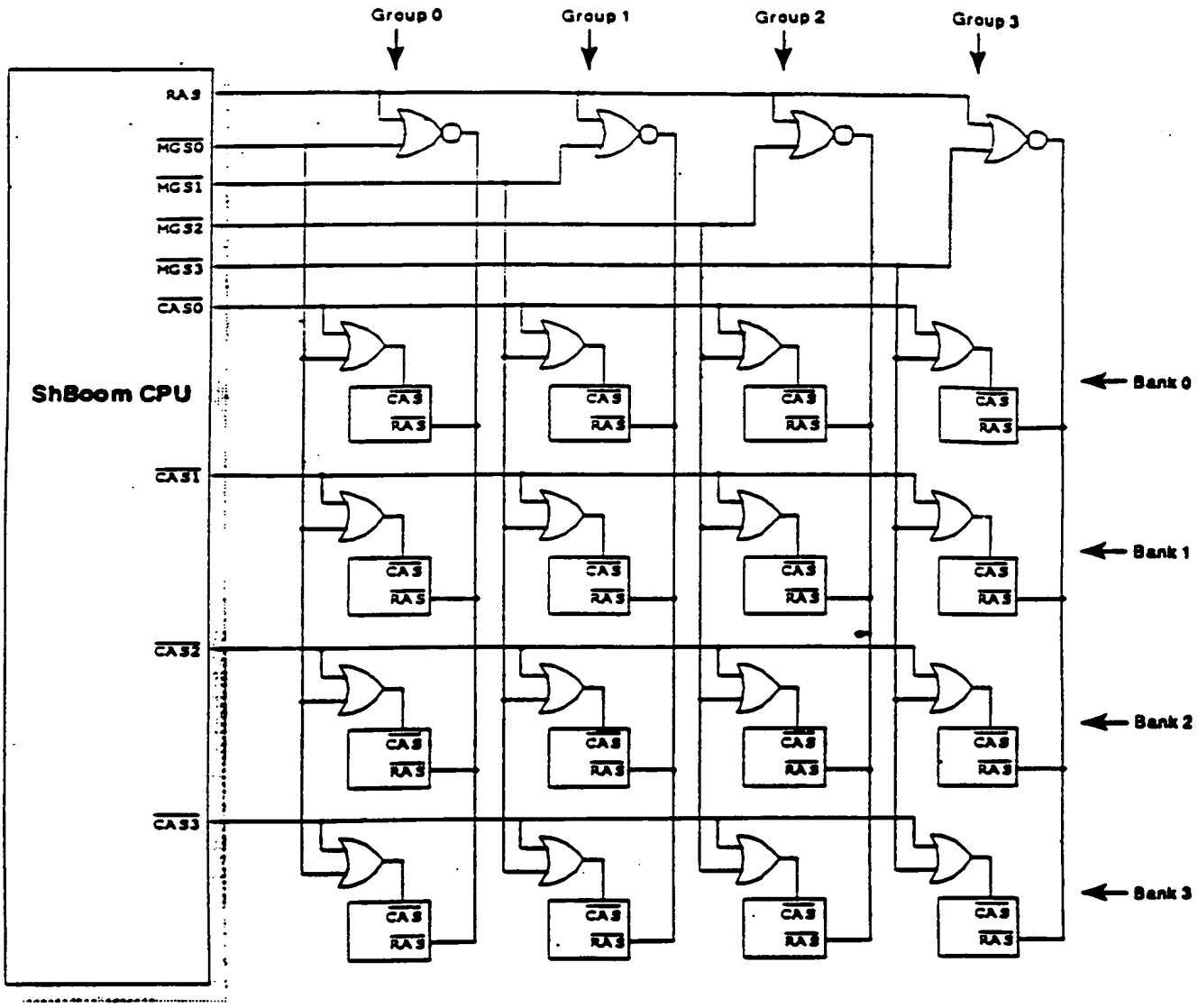
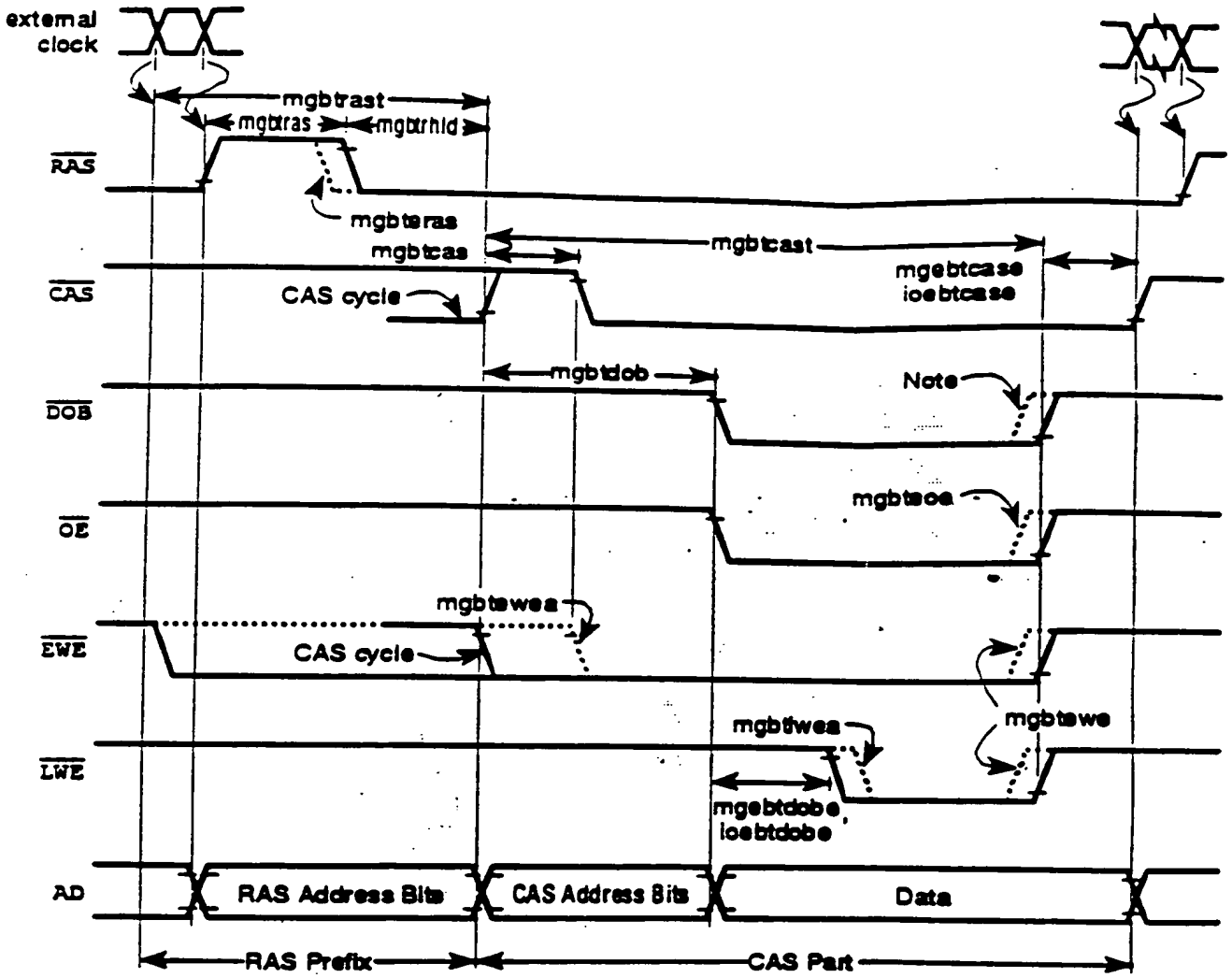


FIG. 18



Note: –DOB rise tracks –OE and –EARLYWE/–LATEWE rise.

FIG. 19

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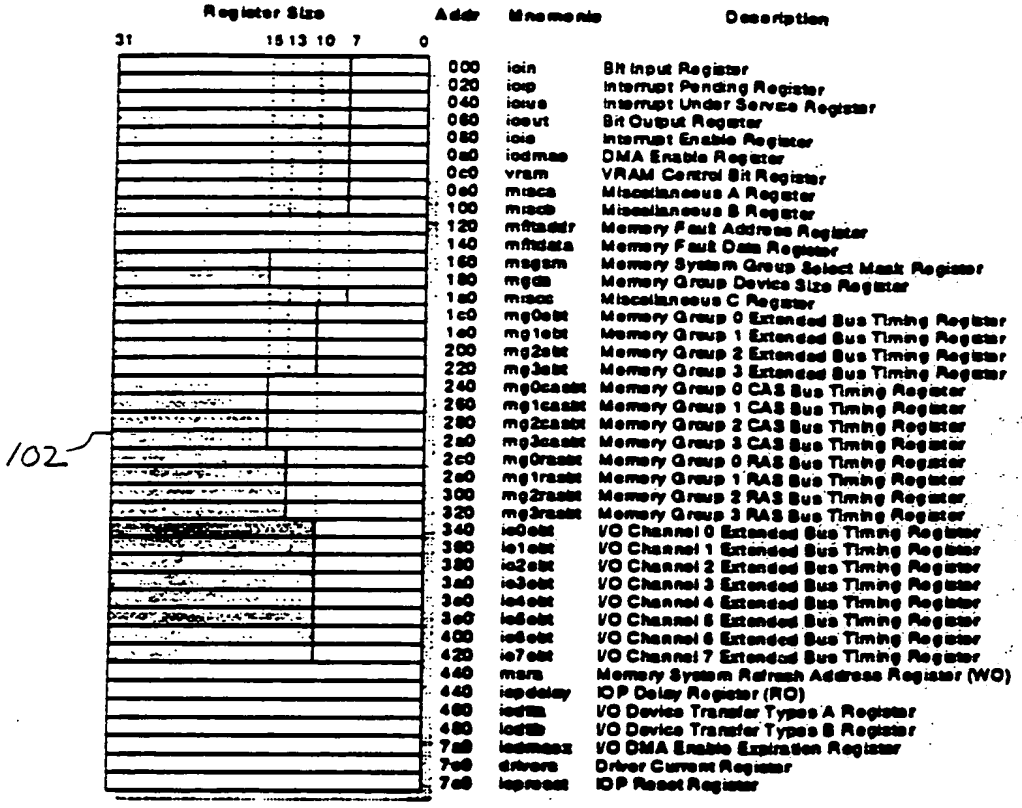
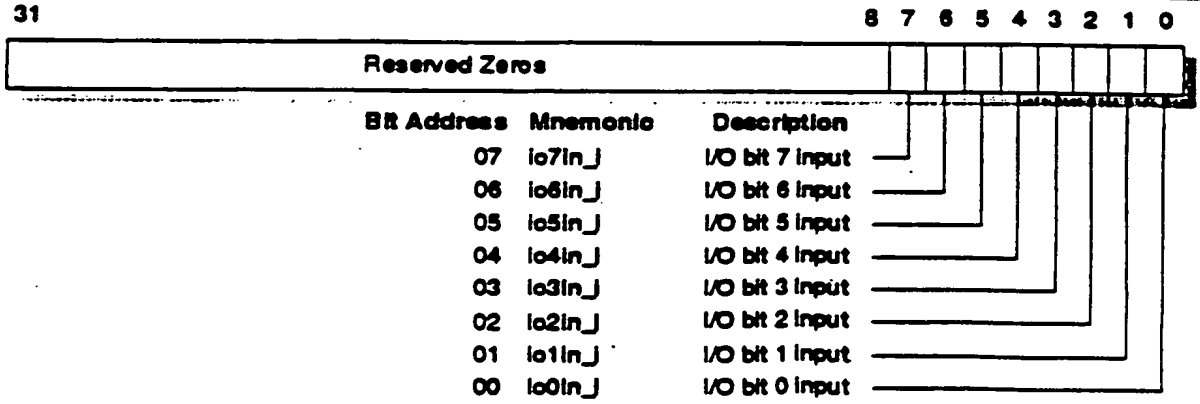


FIG. 20

000 ioin Bit Input Register



Bit Address	Mnemonic	Description
07	io7in_j	I/O bit 7 input
06	io6in_j	I/O bit 6 input
05	io5in_j	I/O bit 5 input
04	io4in_j	I/O bit 4 input
03	io3in_j	I/O bit 3 input
02	io2in_j	I/O bit 2 input
01	io1in_j	I/O bit 1 input
00	io0in_j	I/O bit 0 input

FIG. 21

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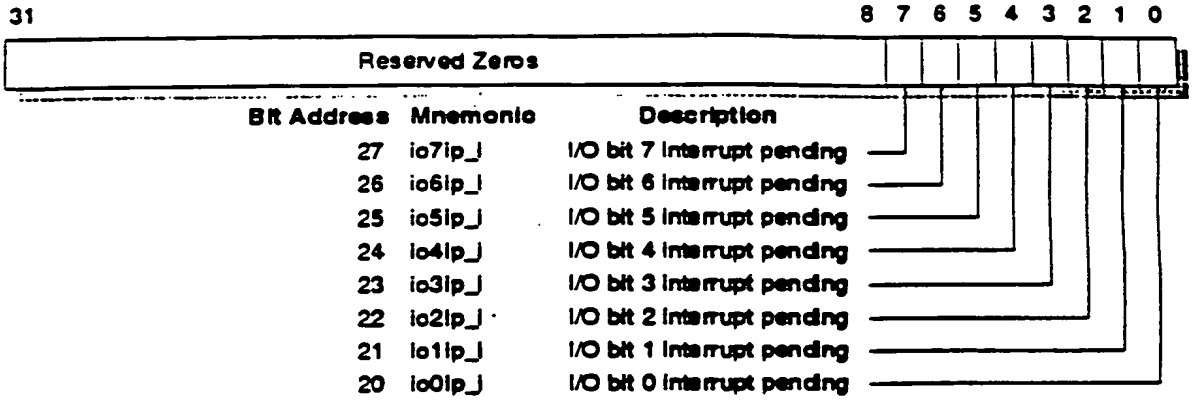
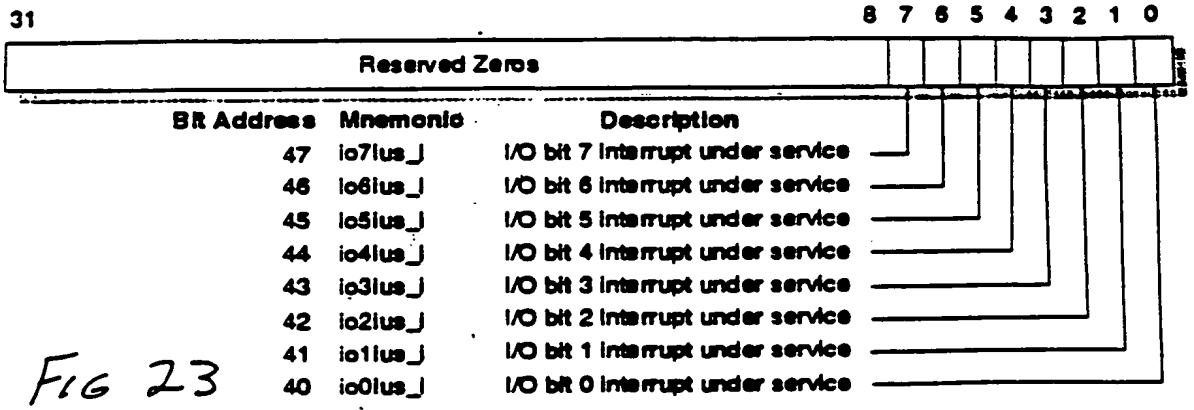
20 ioip Interrupt Pending Register



Bit Address	Mnemonic	Description
27	io7ip_l	I/O bit 7 interrupt pending
26	io6ip_l	I/O bit 6 interrupt pending
25	io5ip_l	I/O bit 5 interrupt pending
24	io4ip_l	I/O bit 4 interrupt pending
23	io3ip_l	I/O bit 3 interrupt pending
22	io2ip_l	I/O bit 2 interrupt pending
21	io1ip_l	I/O bit 1 interrupt pending
20	io0ip_l	I/O bit 0 interrupt pending

FIG. 22

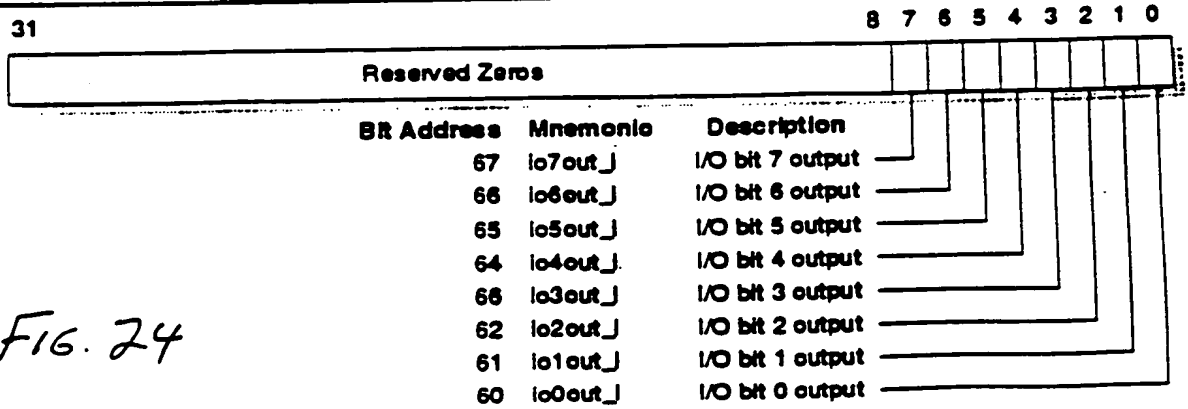
40 ioius Interrupt Under Service Register



Bit Address	Mnemonic	Description
47	io7ius_l	I/O bit 7 interrupt under service
46	io6ius_l	I/O bit 6 interrupt under service
45	io5ius_l	I/O bit 5 interrupt under service
44	io4ius_l	I/O bit 4 interrupt under service
43	io3ius_l	I/O bit 3 interrupt under service
42	io2ius_l	I/O bit 2 interrupt under service
41	io1ius_l	I/O bit 1 interrupt under service
40	io0ius_l	I/O bit 0 interrupt under service

FIG 23

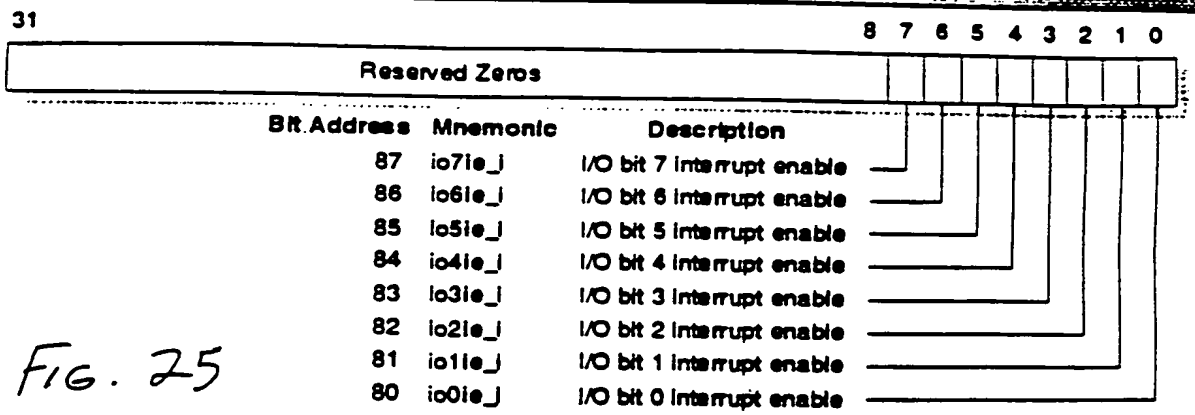
60 iocout Bit Output Register



Bit Address	Mnemonic	Description
67	io7out_l	I/O bit 7 output
66	io6out_l	I/O bit 6 output
65	io5out_l	I/O bit 5 output
64	io4out_l	I/O bit 4 output
66	io3out_l	I/O bit 3 output
62	io2out_l	I/O bit 2 output
61	io1out_l	I/O bit 1 output
60	io0out_l	I/O bit 0 output

FIG. 24

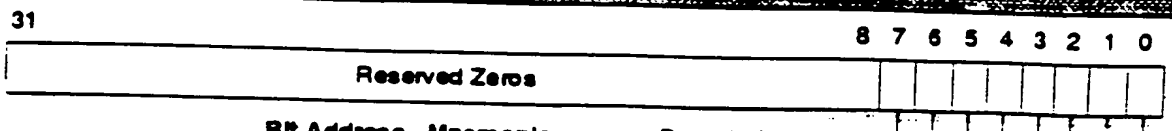
80 ioie — Interrupt Enable Register



Bit Address	Mnemonic	Description
87	io7ie_l	I/O bit 7 interrupt enable
86	io6ie_l	I/O bit 6 interrupt enable
85	io5ie_l	I/O bit 5 interrupt enable
84	io4ie_l	I/O bit 4 interrupt enable
83	io3ie_l	I/O bit 3 interrupt enable
82	io2ie_l	I/O bit 2 interrupt enable
81	io1ie_l	I/O bit 1 interrupt enable
80	io0ie_l	I/O bit 0 interrupt enable

FIG. 25

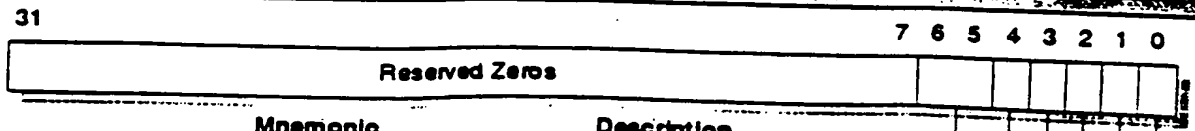
A0 iodmae — DMA Enable Register



Bit Address	Mnemonic	Description
A7	io7dmae_l	I/O bit 7 DMA enable
A6	io6dmae_l	I/O bit 6 DMA enable
A5	io5dmae_l	I/O bit 5 DMA enable
A4	io4dmae_l	I/O bit 4 DMA enable
A3	io3dmae_l	I/O bit 3 DMA enable
A2	io2dmae_l	I/O bit 2 DMA enable
A1	io1dmae_l	I/O bit 1 DMA enable
A0	io0dmae_l	I/O bit 0 DMA enable

FIG. 26

C0 vram — VRAM Control Bit Register



Mnemonic	Description
msvgrp	memory system VRAM group
dsfvcas	state of $\overline{DSF}$ at VRAM $\overline{CAS}$ fall
dsfvras	state of $\overline{DSF}$ at next VRAM $\overline{RAS}$ fall
casbvras	$\overline{CAS}$ fall before $\overline{RAS}$ next VRAM RAS
wevras	$\overline{WE}$ low at next VRAM $\overline{RAS}$ fall
oevras	$\overline{OE}$ low at next VRAM $\overline{RAS}$ fall

FIG. 27

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E0 misca Miscellaneous A Register

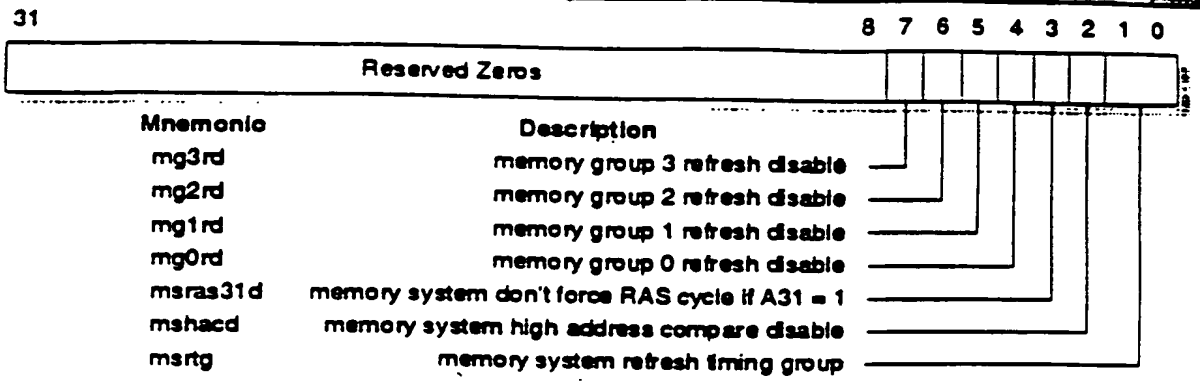


FIG. 28

100 misob Miscellaneous B Register

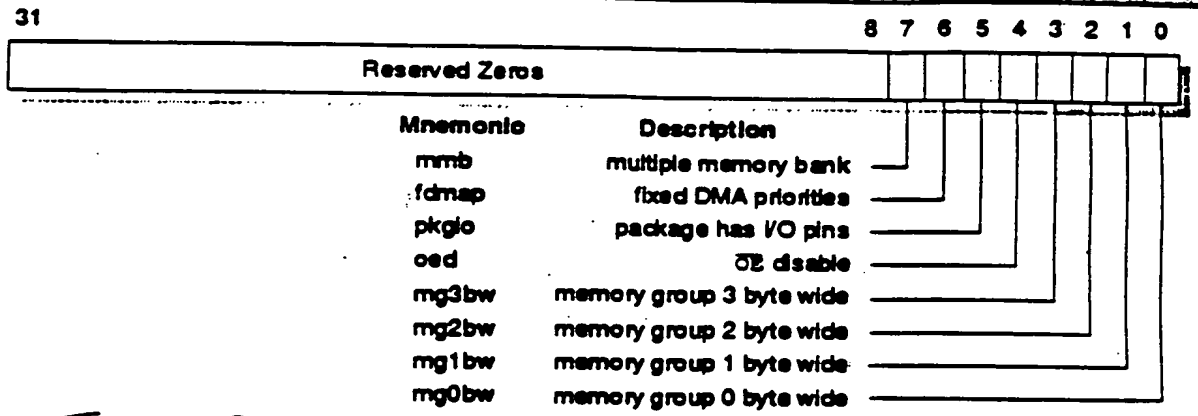
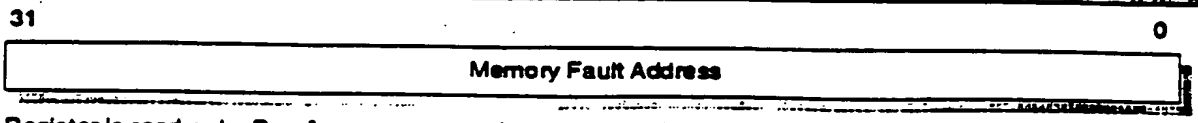


FIG. 29

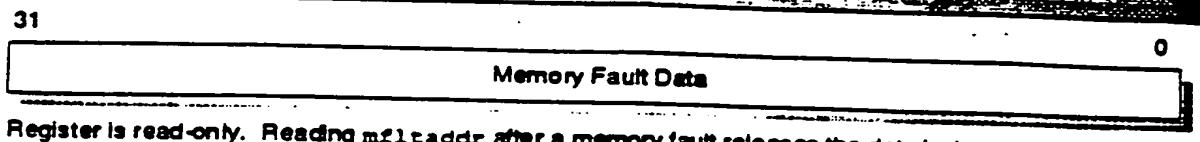
120 mfltaddr Memory Fault Address Register



Register is read-only. Reading `mfltaddr` after a memory fault releases the data lock on `mfltaddr` and `mfltdata`, allowing data to flow into the registers.

FIG. 30

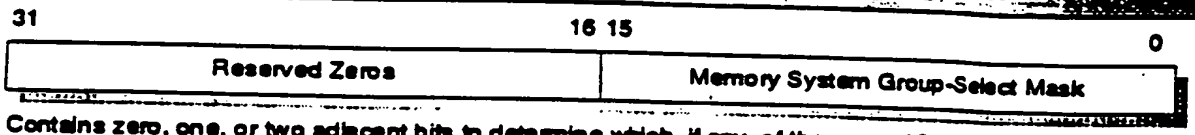
140 mfltdata Memory Fault Data Register



Register is read-only. Reading `mfltaddr` after a memory fault releases the data lock on `mfltaddr` and `mfltdata`, allowing data to flow into the registers.

FIG. 31

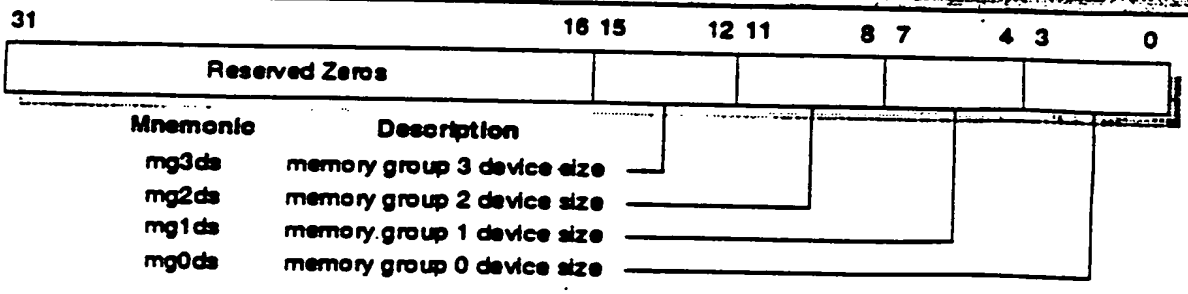
160 msgsm Memory System Group Select Mask Register



Contains zero, one, or two adjacent bits to determine which, if any, of the upper 16 address bits will be decoded to select memory groups.

FIG. 32

180 mgds Memory Group Device Size Register



Device Sizes

0x00	64K DRAM	0x04	1M DRAM	0x08	8M DRAM	0x0c	64M DRAM (asym)
0x01	128K DRAM	0x05	2M DRAM	0x09	16M DRAM (asym)	0x0d	64M DRAM
0x02	256K DRAM	0x06	4M DRAM (asym)	0x0a	16M DRAM	0x0e	128M DRAM
0x03	512K DRAM	0x07	4M DRAM	0x0b	32M DRAM	0x0f	SRAM

FIG. 33

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1A0 misco Miscellaneous C Register

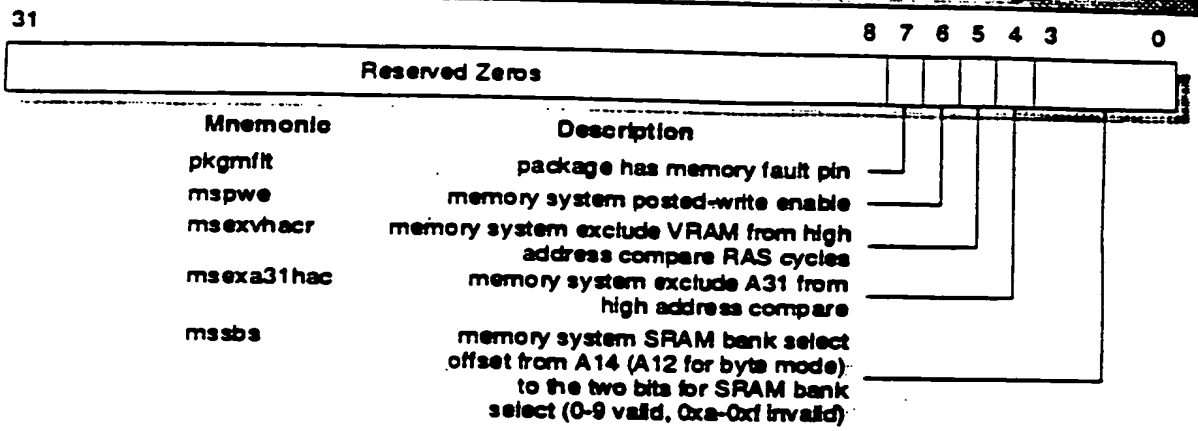


FIG. 34

mgXebt Memory Group 0–3 Extended Bus Timing Registers

1C0 mg0ebt 1E0 mg1ebt 200 mg2ebt 220 mg3ebt

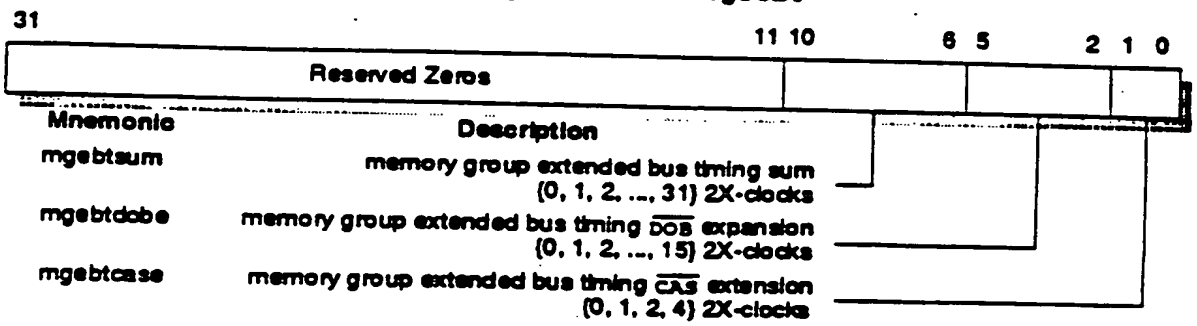
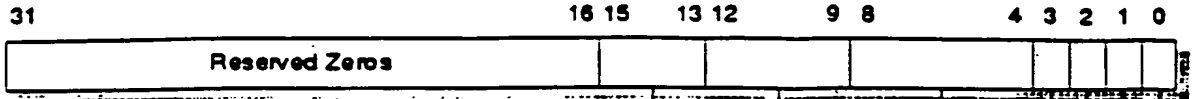


FIG. 35

mgXcasbt Memory Group 0–3 CAS Bus Timing Registers

240 mg0casbt 260 mg1casbt 280 mg2casbt 2A0 mg3casbt

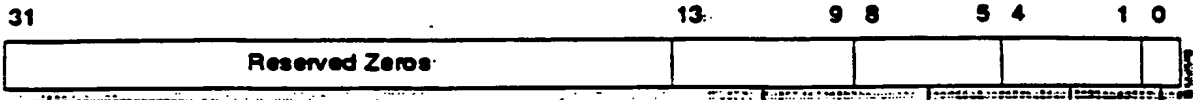


Mnemonic	Description
mgbtcas	memory group bus timing $\overline{CAS}$ low start (1, 2, 3, ..., 8) 4X-clock cycles
mgbtdob	memory group bus timing $\overline{DOB}$ low start (1, 2, 3, ..., 16) 4X-clock cycles
mgbtcast	memory group bus timing $\overline{CAS}$ cycle total (1, 2, 3, ..., 32) 2X-clock cycles
mgbtewea	memory group bus timing late fall $\overline{EWE}$ active (0=active at cycle start, 1=active at $\overline{CAS}$ low)
mgbtwea	memory group bus timing $\overline{EWE}$ active, delay by one 4X-clock cycle
mgbteoe	memory group bus timing early rise $\overline{OE}$ by one 4X-clock cycle
mgbtewe	memory group bus timing early rise write enables by one 4X-clock cycle

FIG. 36

mgXrasbt Memory Group 0–3 RAS Bus Timing Registers

2C0 mg0rasbt 2E0 mg1rasbt 300 mg2rasbt 320 mg3rasbt



Mnemonic	Description
mgbtrast	memory group bus timing RAS prefix cycle total + 1 (0, 1, 2, ..., 31) 2X-clock cycles
mgbtras	memory group bus timing $\overline{RAS}$ low start (1, 2, 3, ..., 16) 2X-clock cycles
mgbtrhld	memory group bus timing row address hold (0, 1, 2, ..., 15) 2X-clock cycles
mgbteras	memory group bus timing early $\overline{RAS}$ low by one 4X-clock cycle

FIG. 37

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loXebt — I/O Channel 0–7 Extended Bus Timing Registers

340 lo0ebt 360 lo1ebt 380 lo2ebt 3A0 lo3ebt
3C0 lo4ebt 3E0 lo5ebt 400 lo6ebt 420 lo7ebt

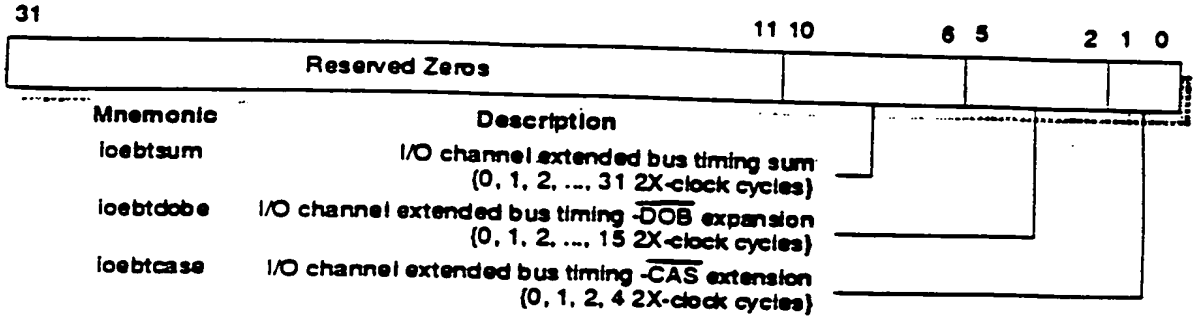

FIG. 38

440 msra — Memory System Refresh Address

WRITE ONLY

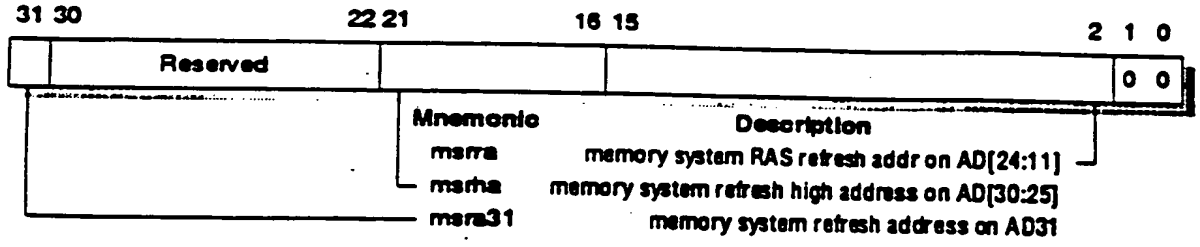

FIG. 39

440 iopdelay — IOP Delay Counter Register

READ ONLY

FIG. 40

460 iodtta I/O Device Transfer Types A Register

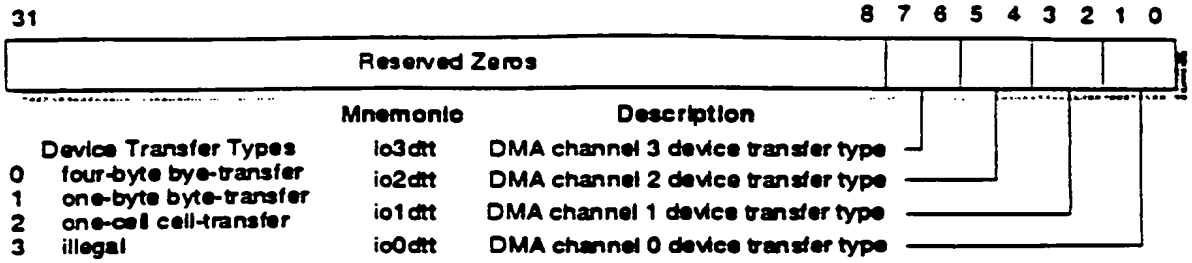

FIG. 41

480 iodttb I/O Device Transfer Types B Register

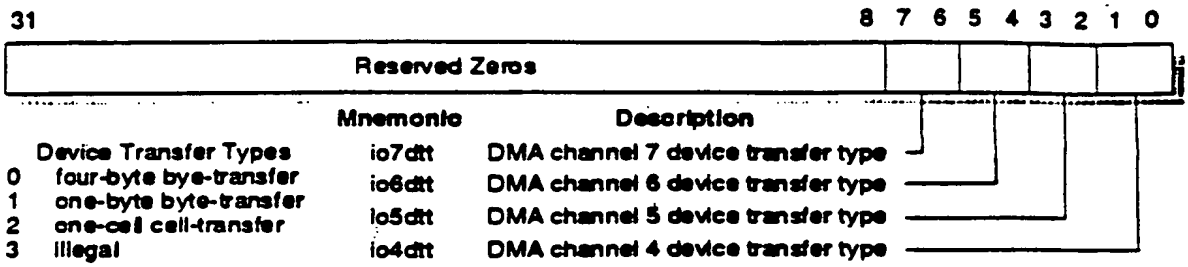

FIG. 42

Reserved Register Addresses

4A0-780

FIG. 43

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7A0 iodmaex DMA Enable Expiration Register

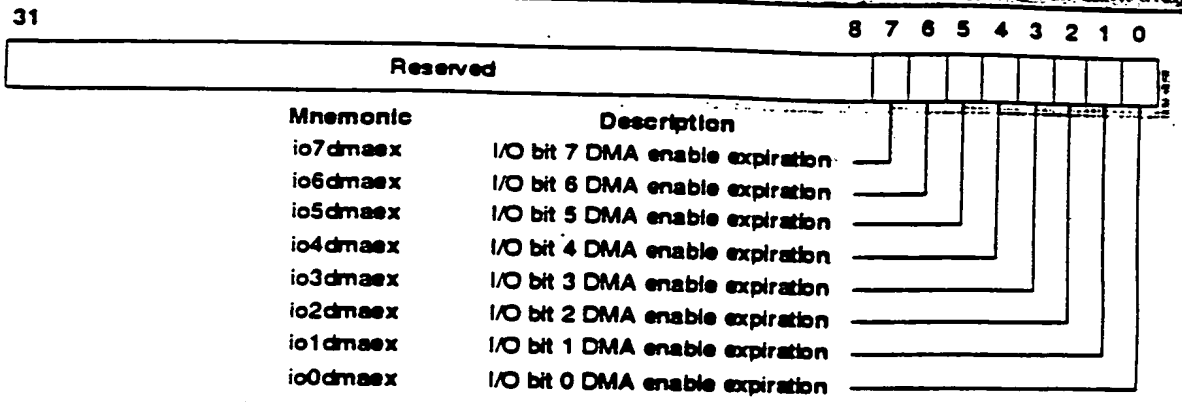
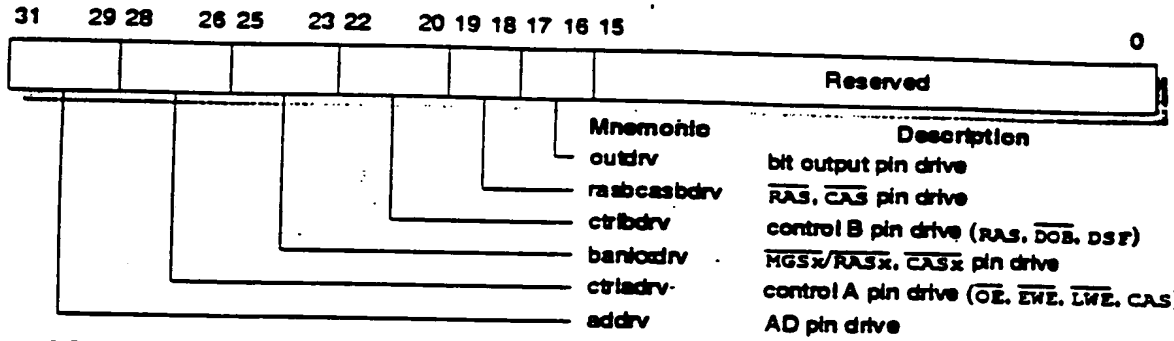


FIG 44

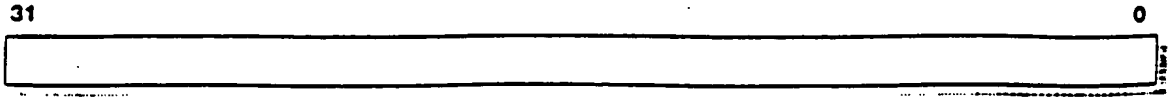
7C0 drivers Driver Current Register



3-Bit Field		2-Bit Field		Where n =	
00n	1 of 3 drivers	0n	1 of 3 drivers	0	1 of 2 pre-drivers
01n	2 of 3 drivers	1n	3 of 3 drivers	1	2 of 2 pre-drivers
11n	3 of 3 drivers				

FIG. 45

7E0 iopreset IOP Reset Register



write	reset IOP on any write
read	0xffffffff while waiting to reset, zero otherwise

FIG. 46

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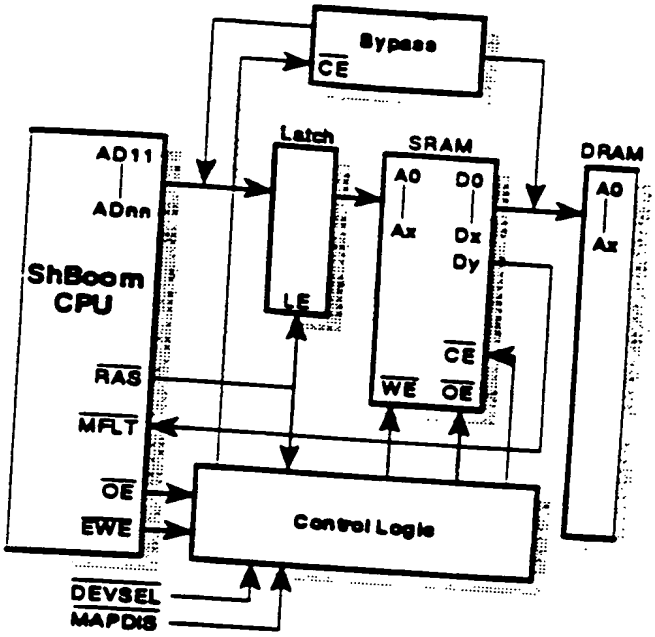
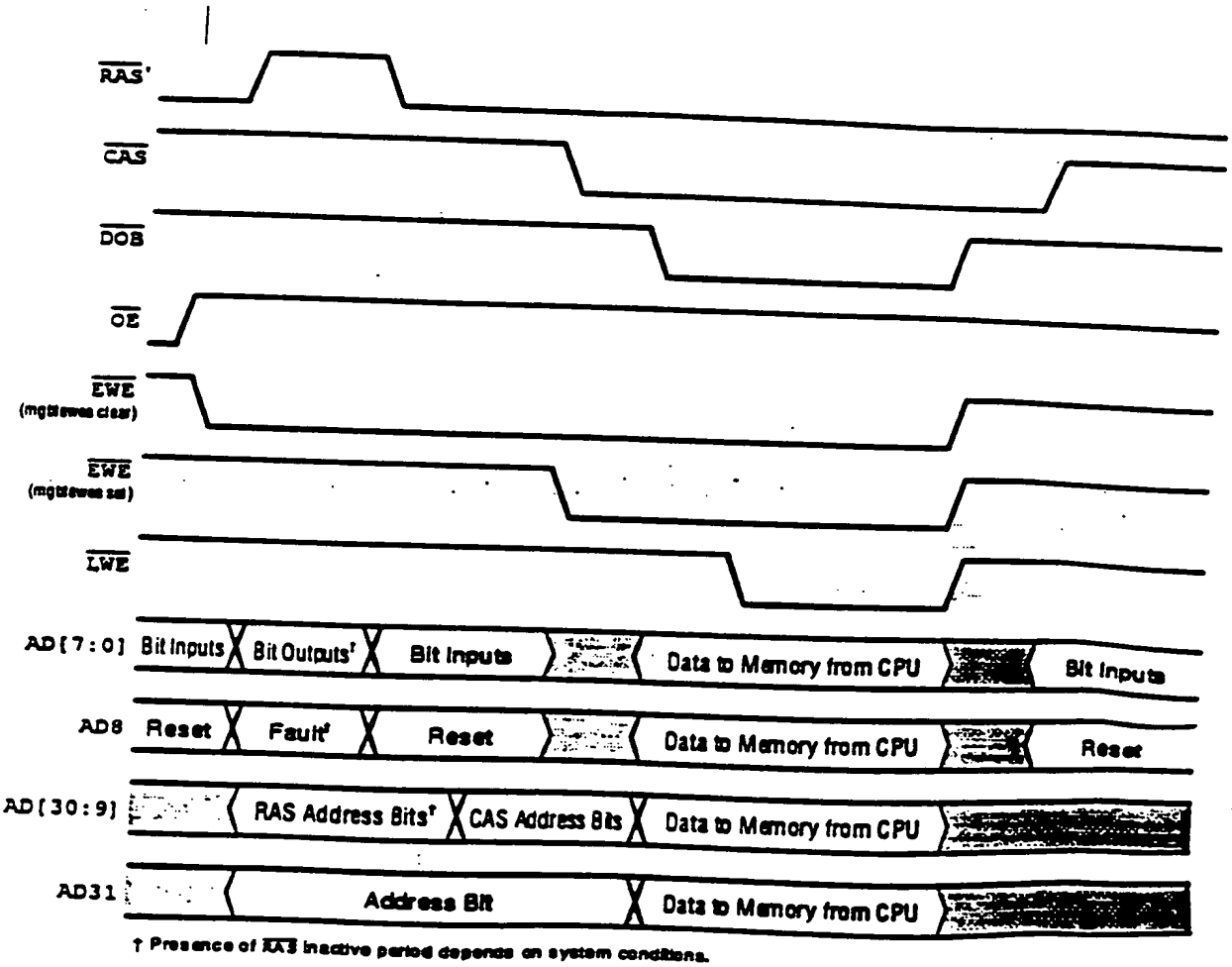
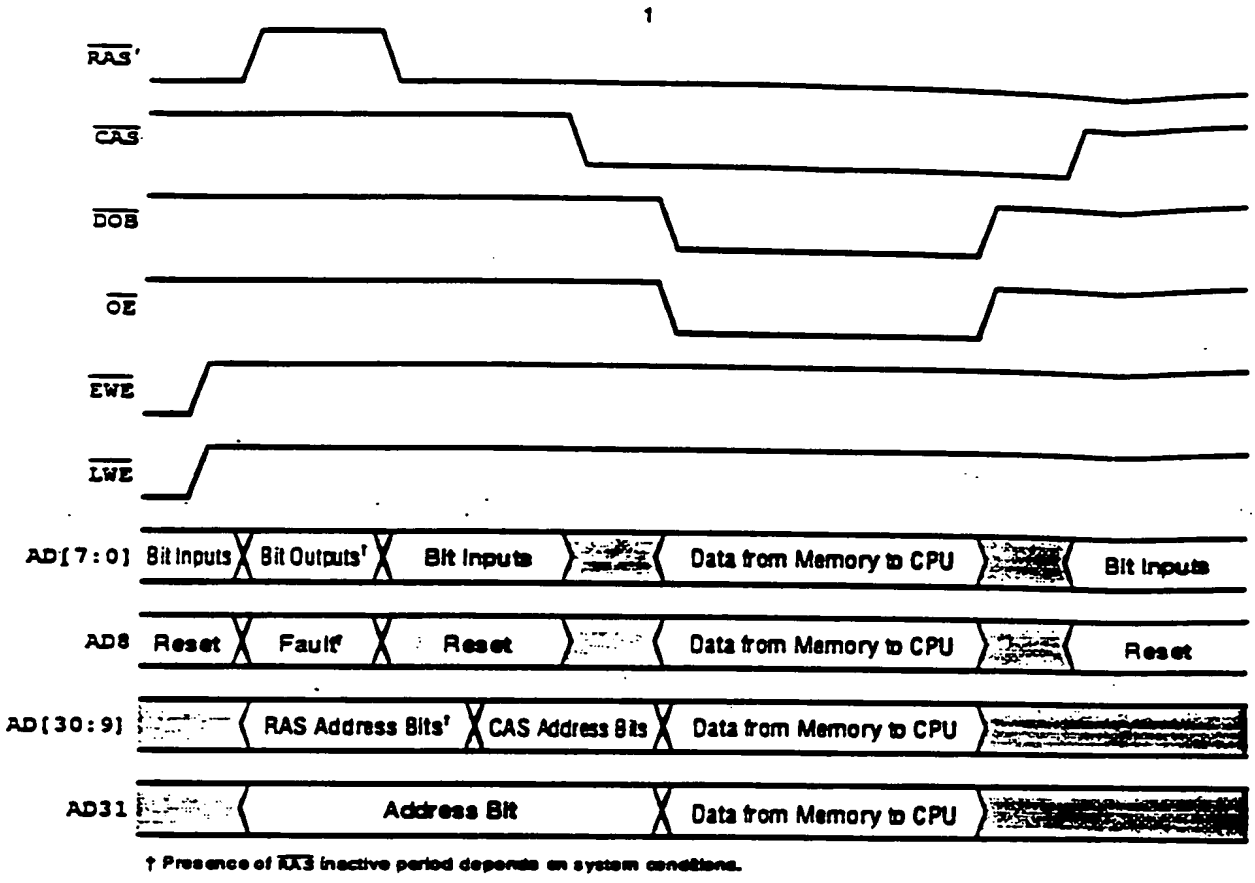


FIG 46a

FIG. 47



† Presence of RAS inactive period depends on system conditions.



† Presence of RAS inactive period depends on system conditions.

FIG 48

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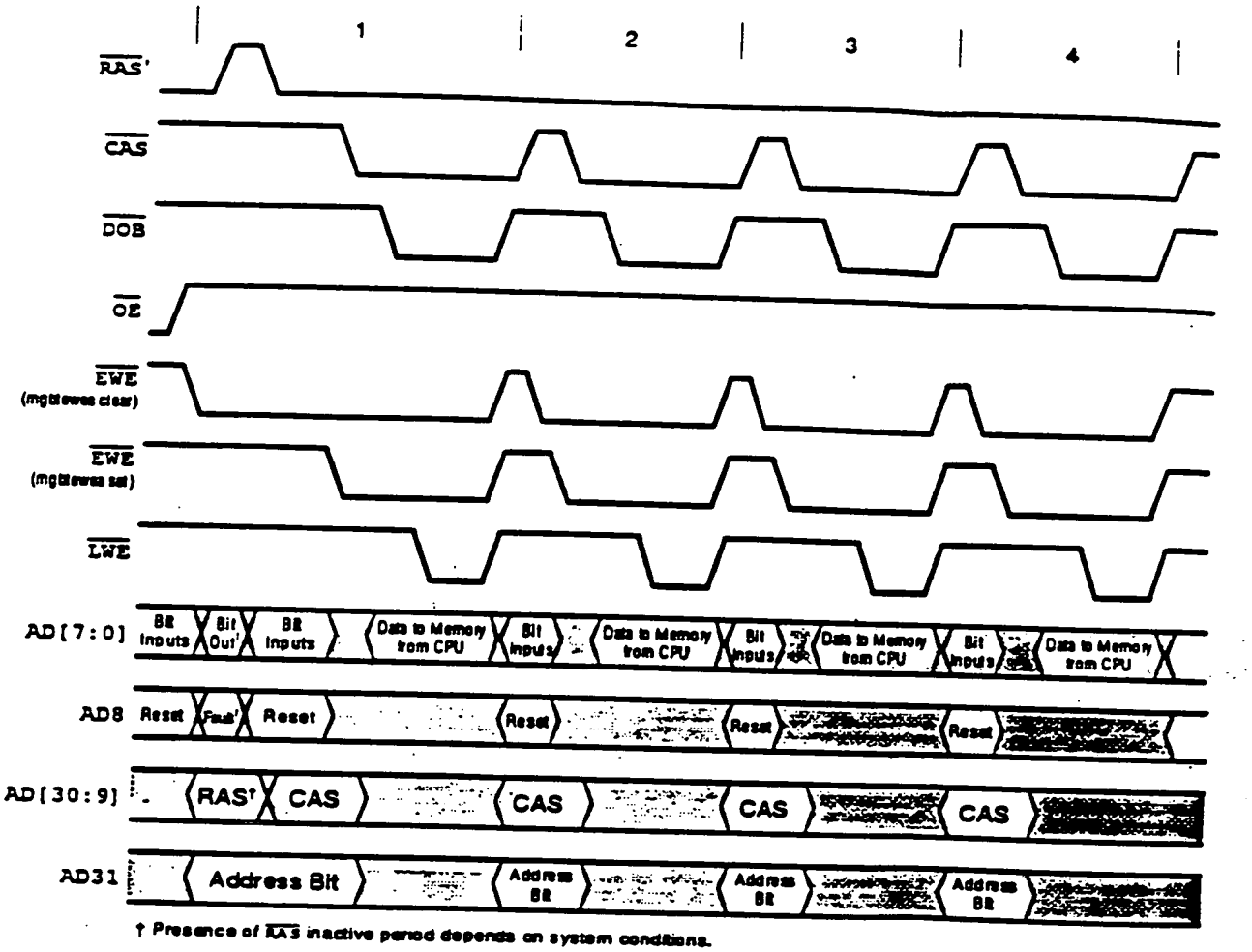


† Presence of $\overline{RAS}$ inactive period depends on system conditions.

FIG. 49

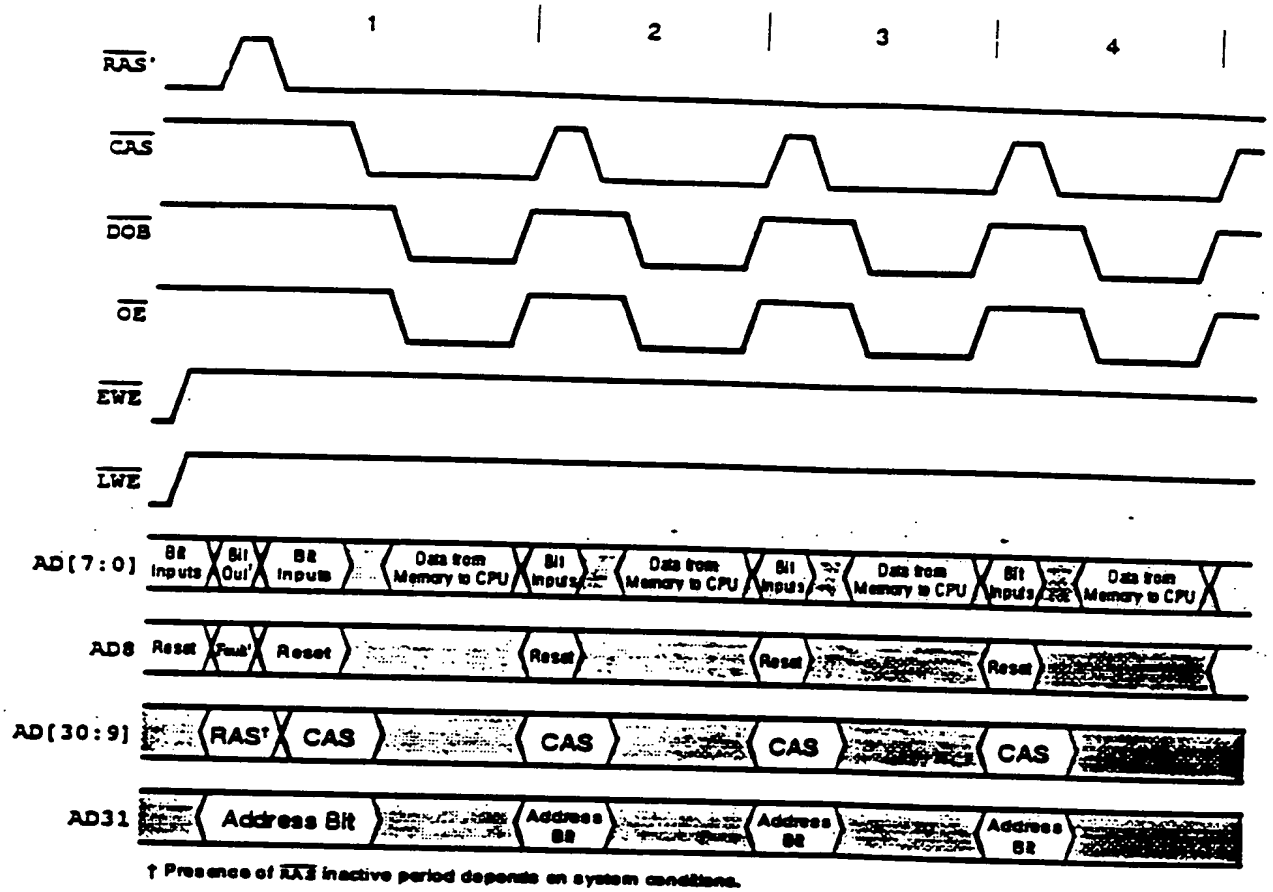
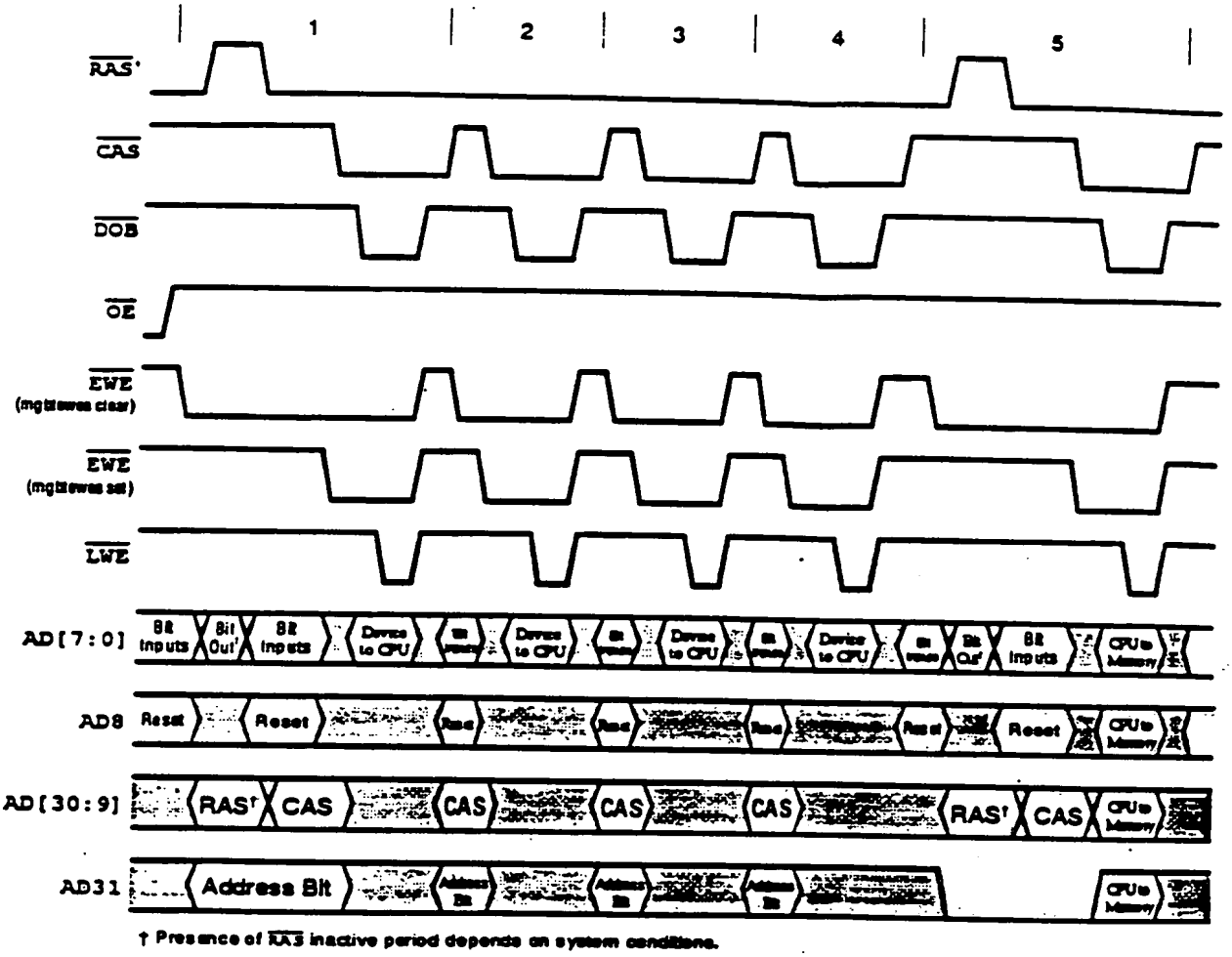


FIG. 50



† Presence of $\overline{RAS}$ inactive period depends on system conditions.

FIG. 51

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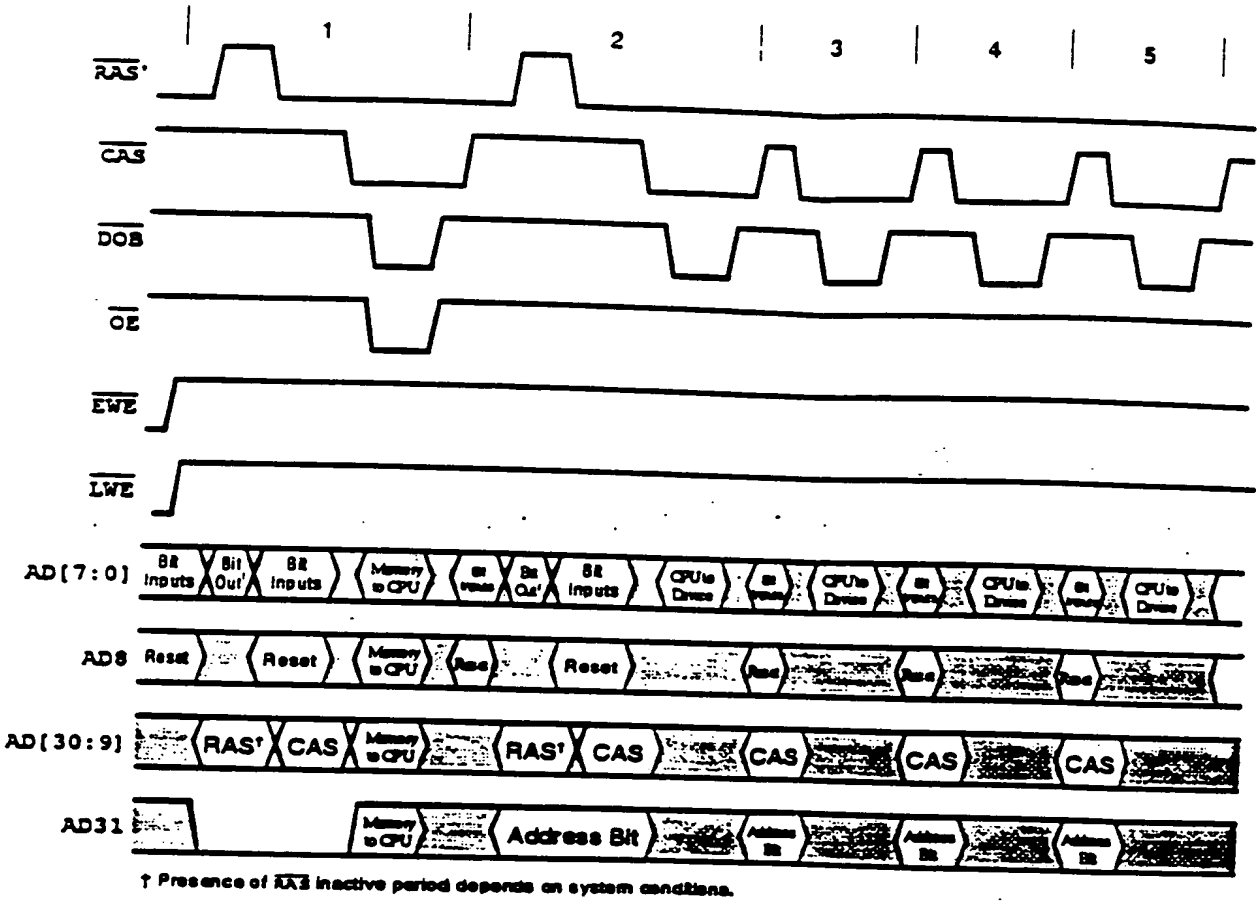


† Presence of $\overline{RAS}$ inactive period depends on system conditions.

FIG. 52

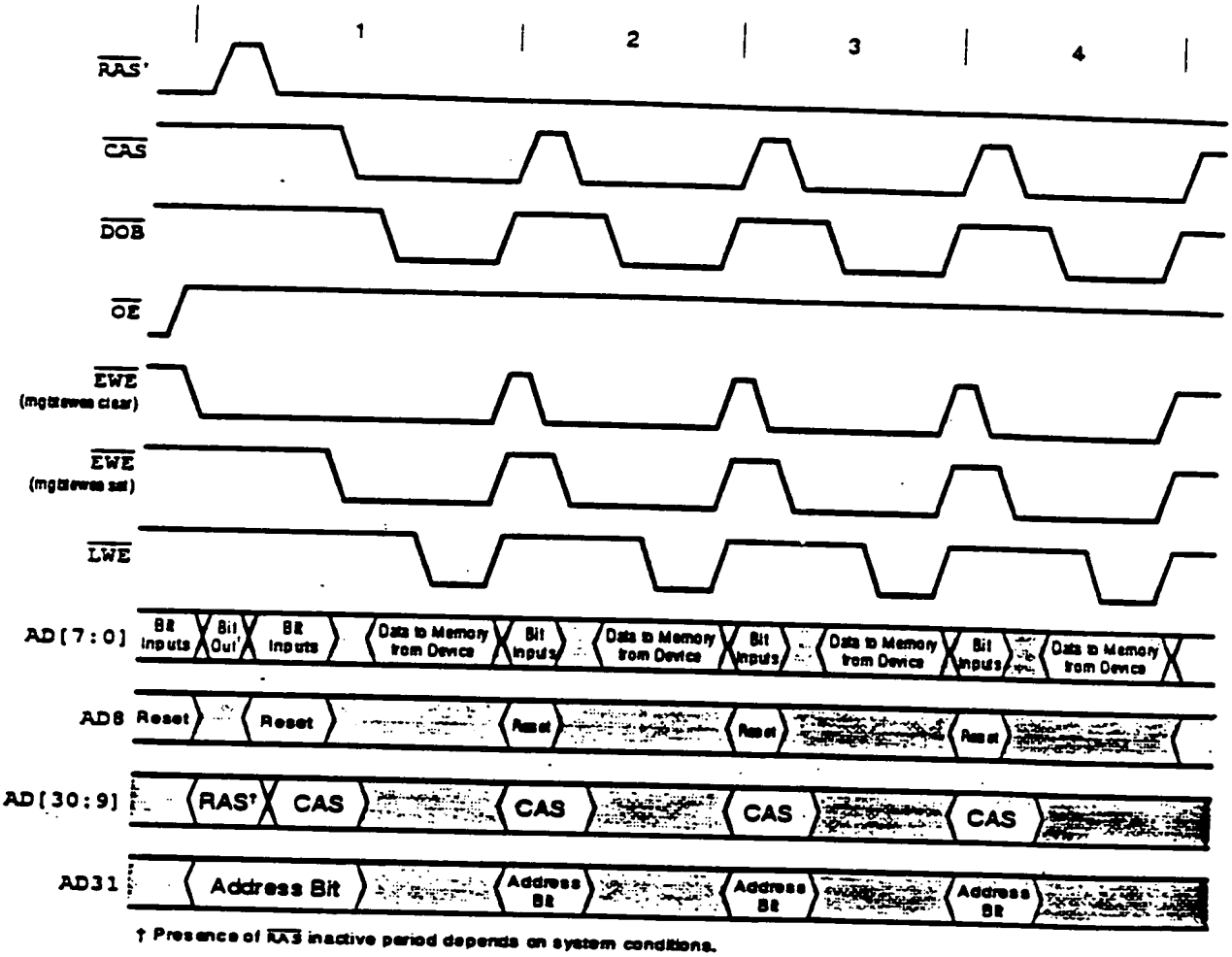
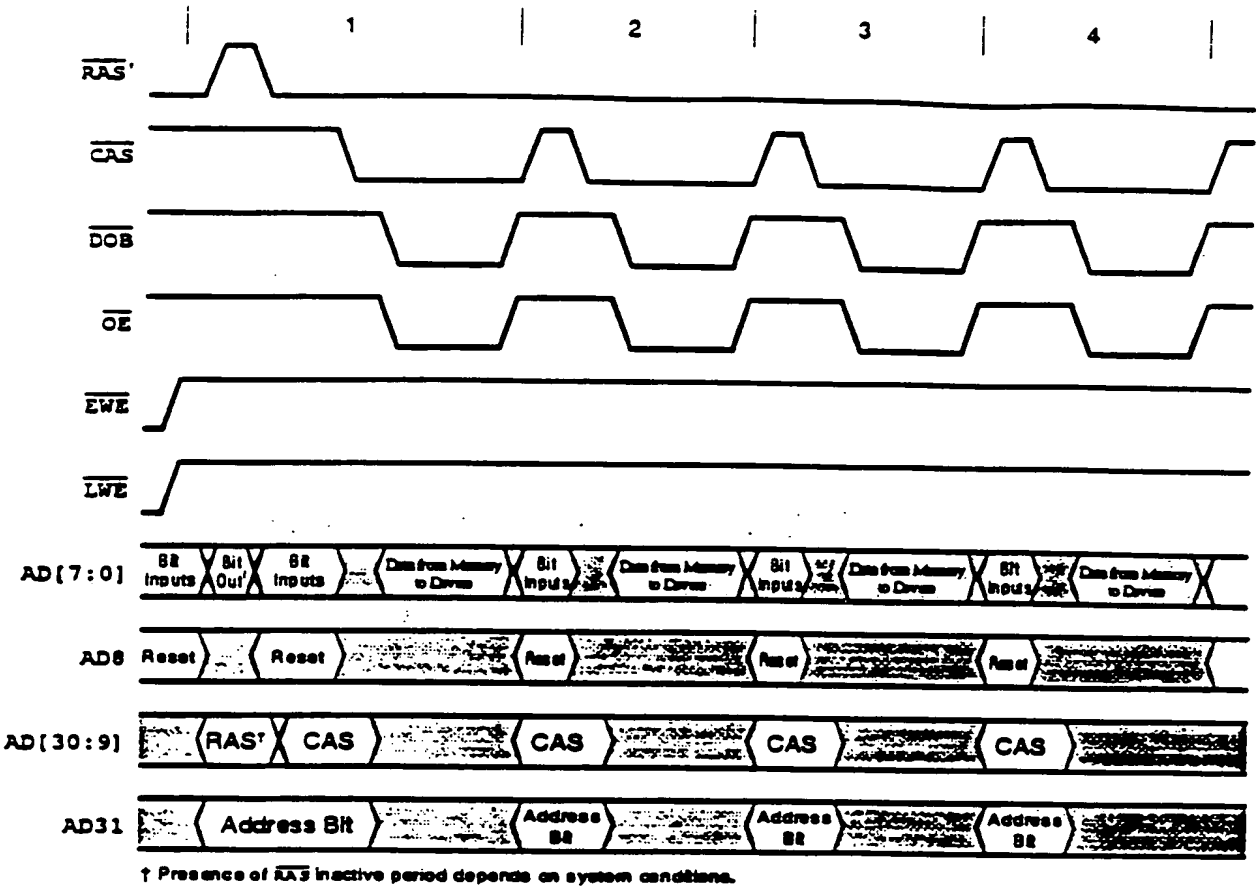

1
2
3
4
RAS'
CAS
DOB
OE
EWE (mgtzewe clear)
EWE (mgtzewe set)
LWE
AD[7:0]
Bit Inputs
Bit Out'
Bit Inputs
Data to Memory from Device
Bit Inputs
Data to Memory from Device
Bit Inputs
Data to Memory from Device
Bit Inputs
Data to Memory from Device
AD8
Reset
Reset
Reset
Reset
Reset
AD[30:9]
RAS†
CAS
CAS
CAS
CAS
AD31
Address Bit
Address Bit
Address Bit
Address Bit
† Presence of RAS inactive period depends on system conditions.

FIG. 53



† Presence of $\overline{RAS}$ inactive period depends on system conditions.

FIG. 54

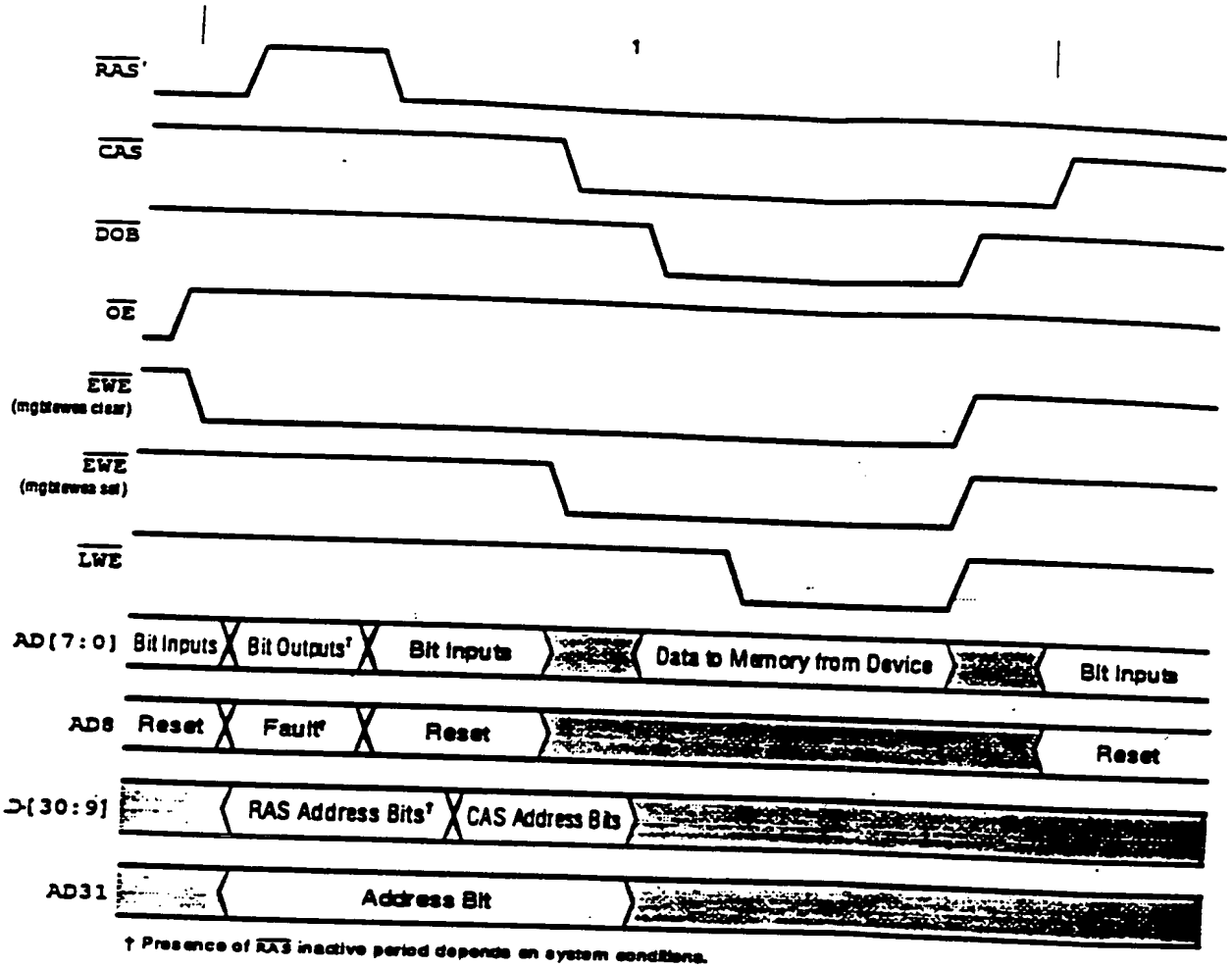


FIG. 55

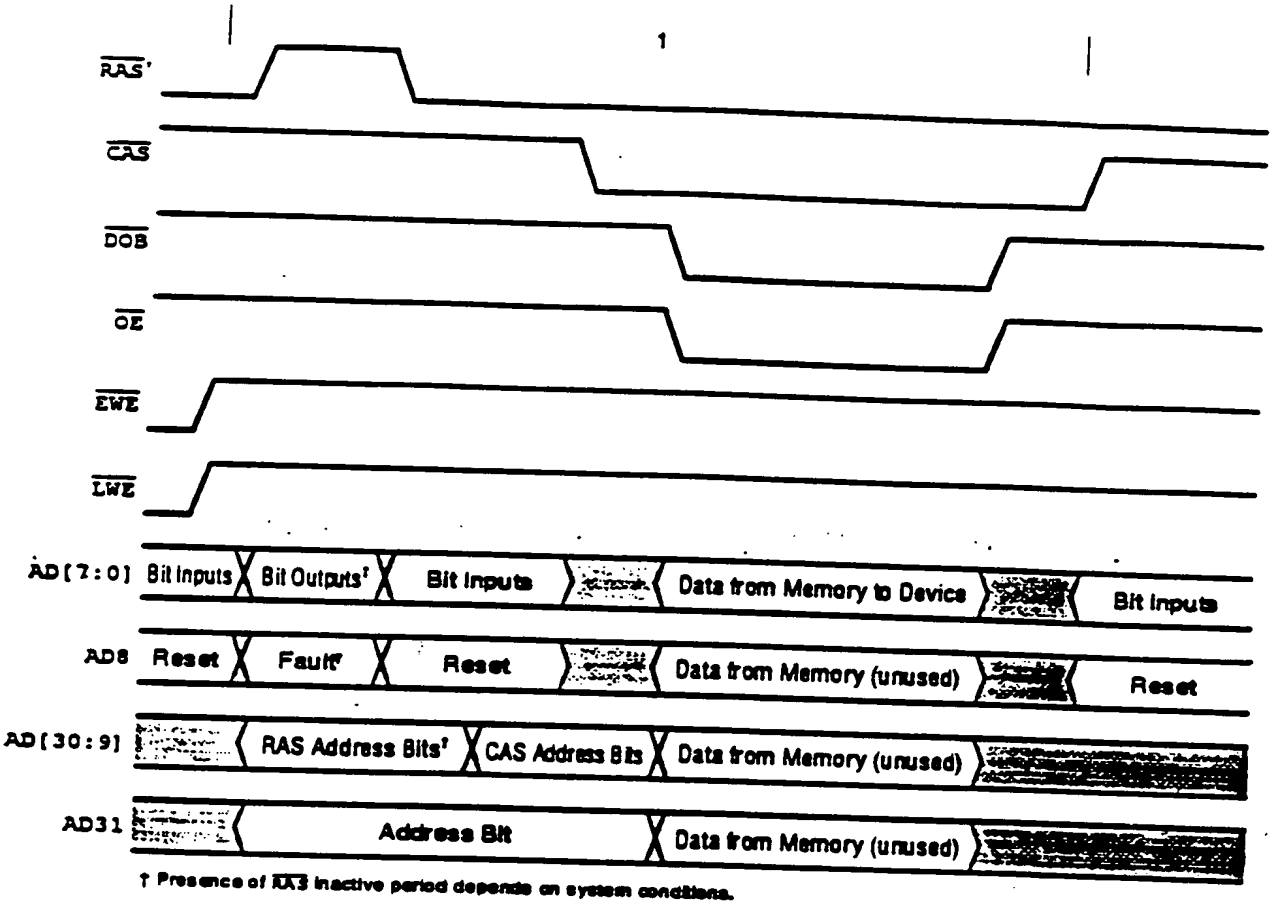


FIG. 56

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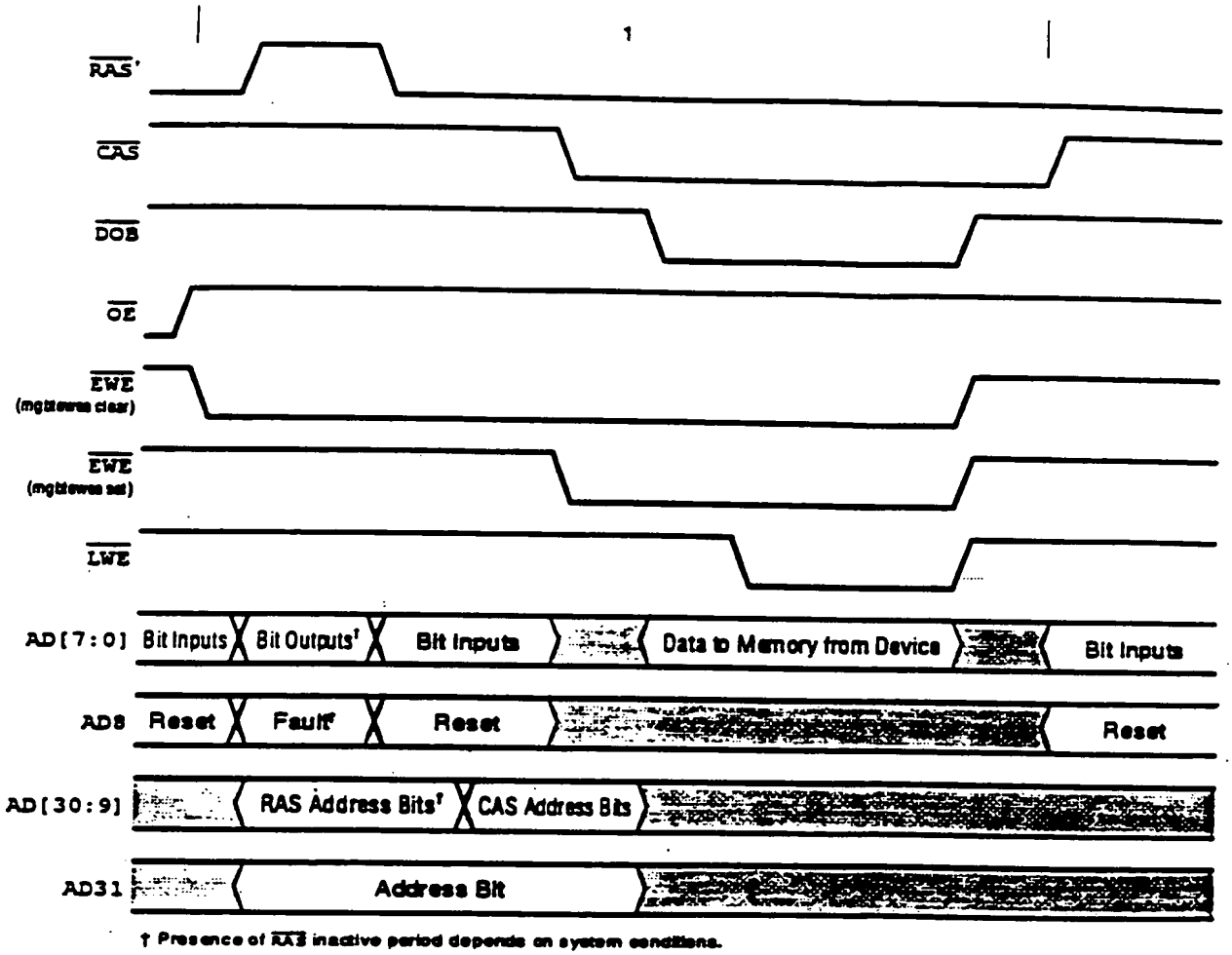

† Presence of RAS inactive period depends on system conditions.

FIG. 57

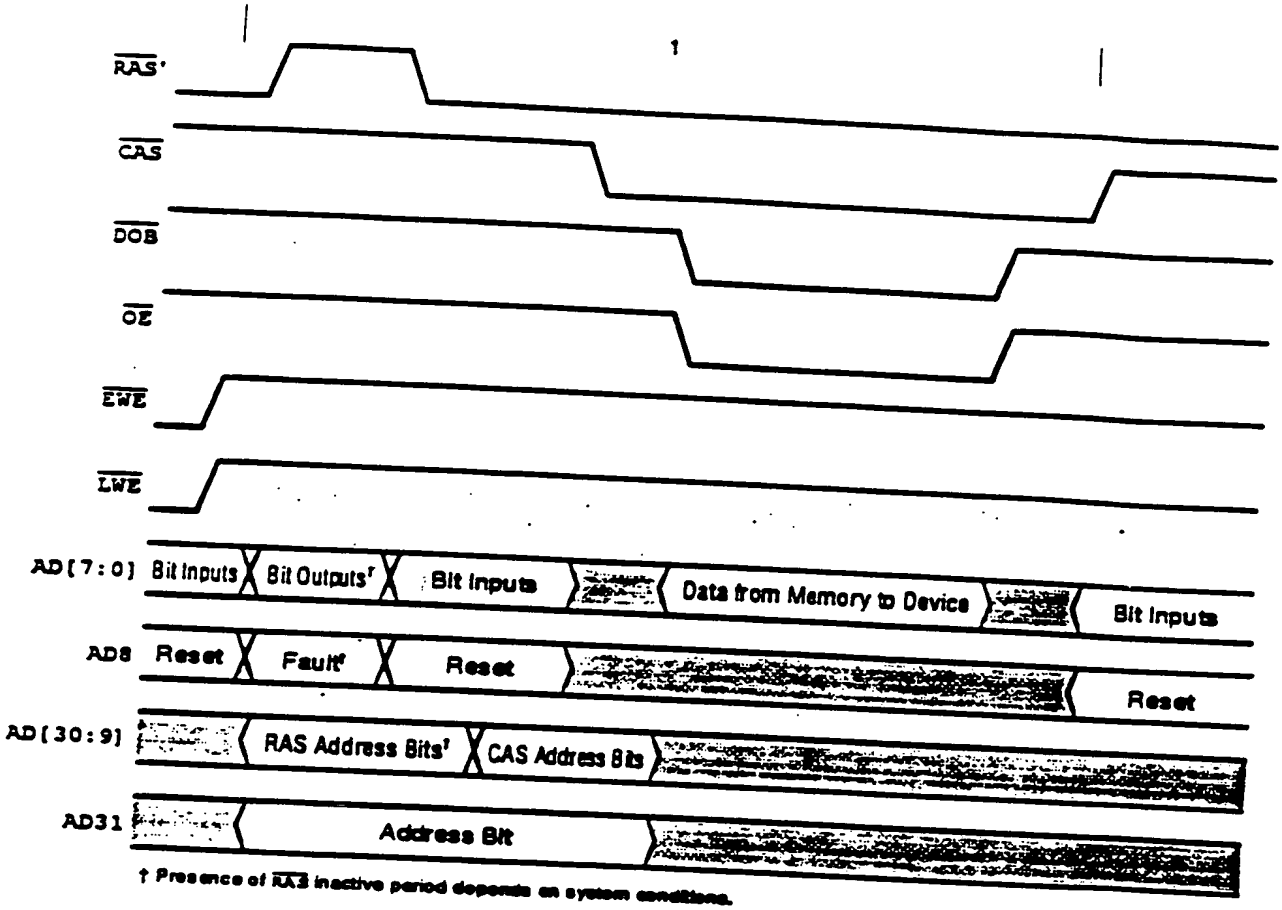

FIG. 58

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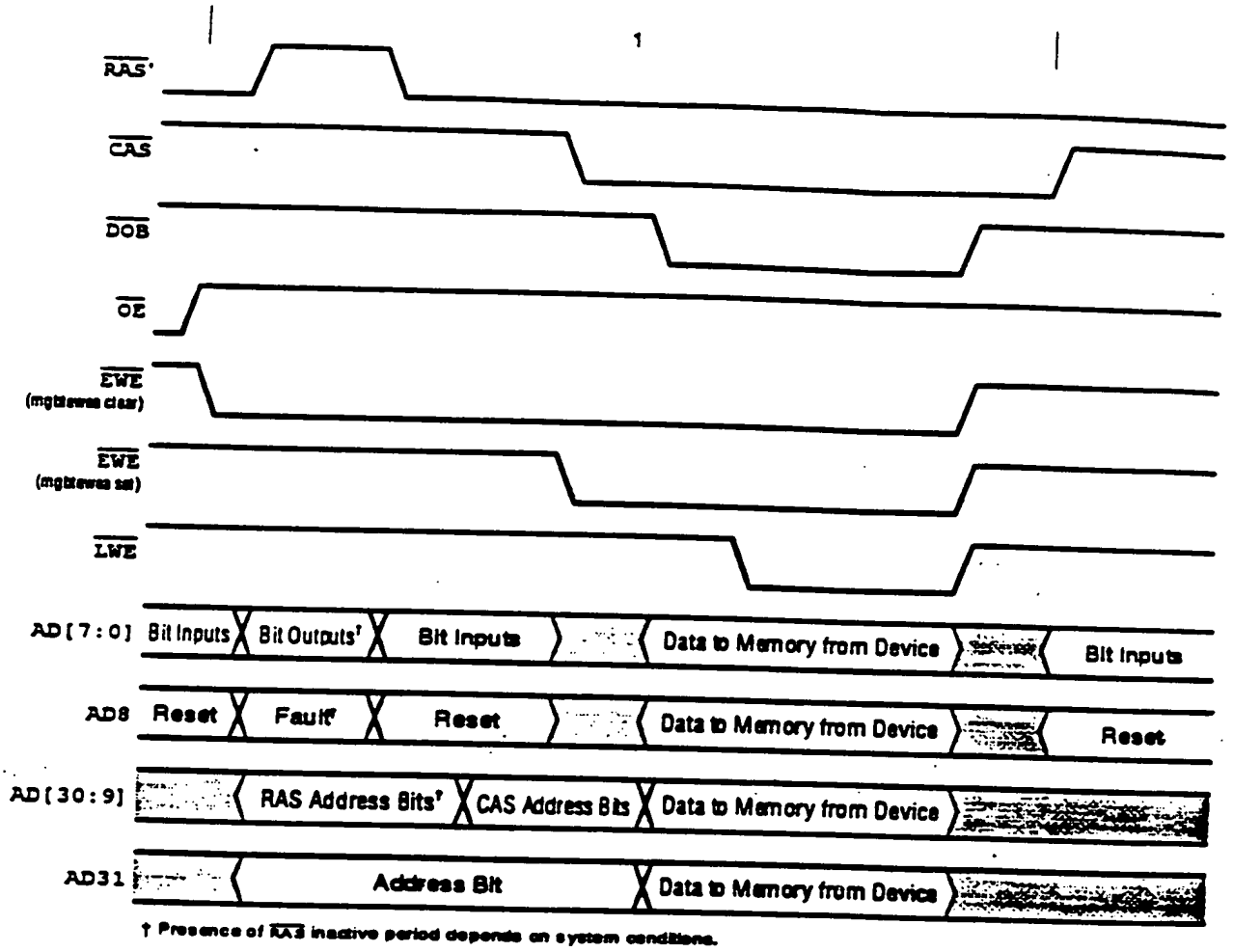

FIG. 59

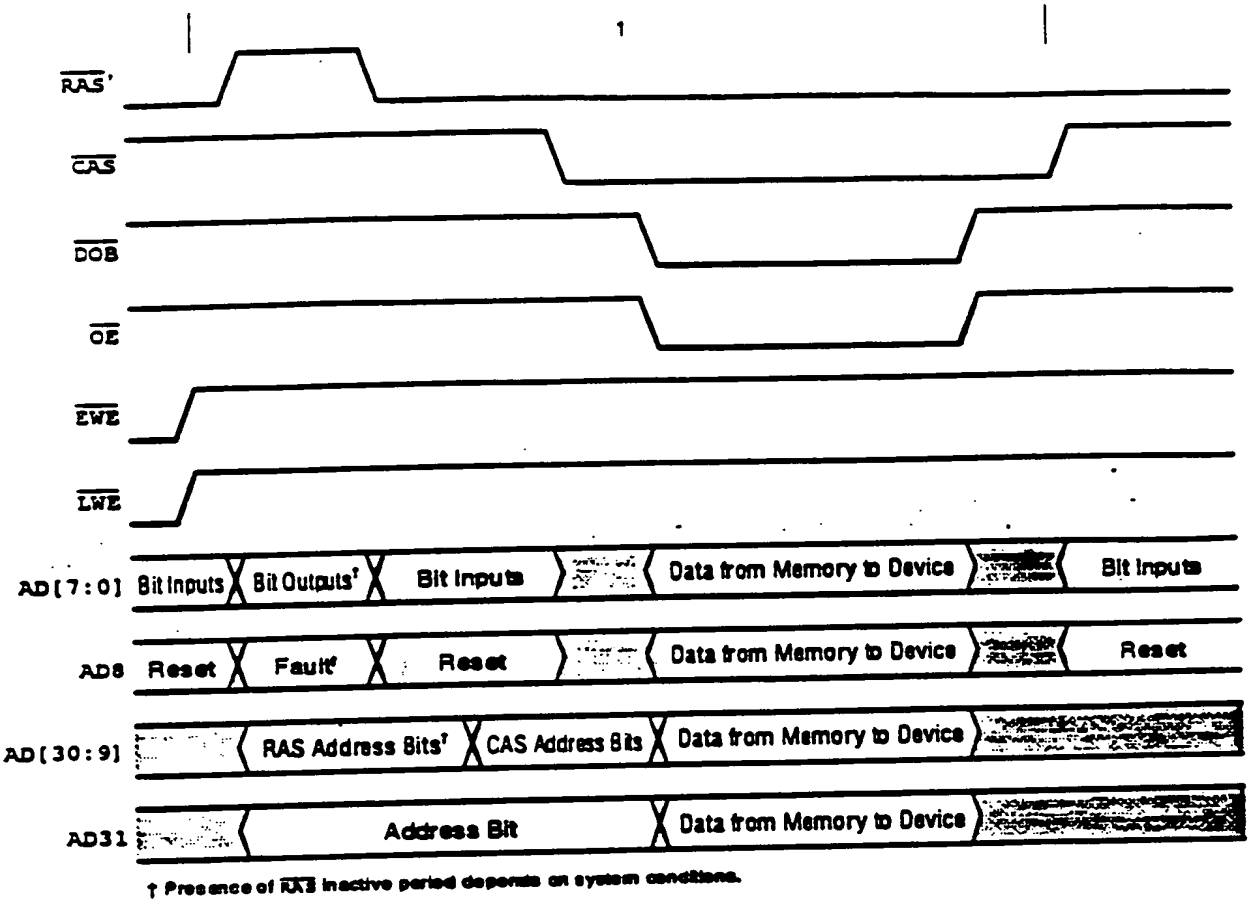

FIG. 60

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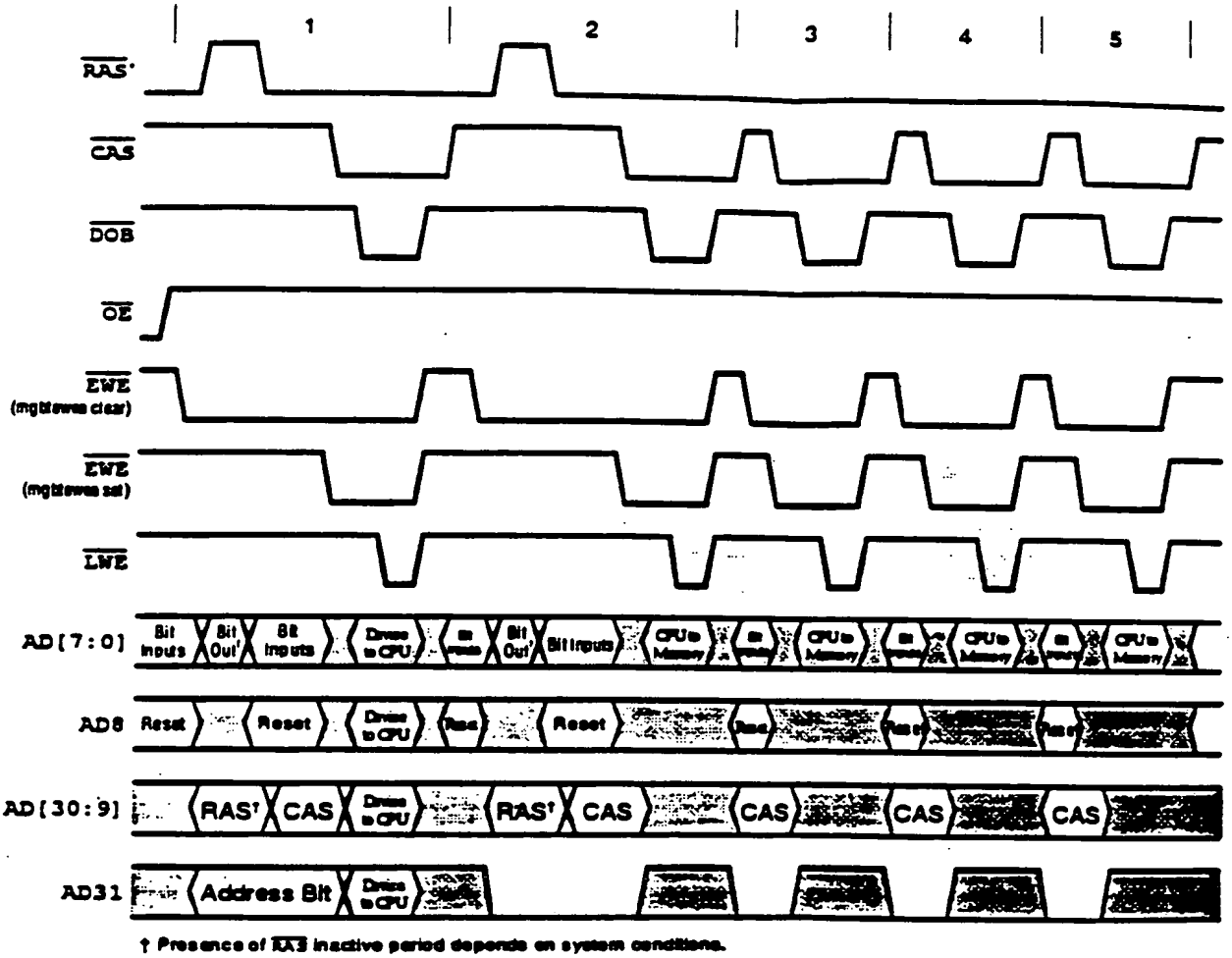

† Presence of RAS inactive period depends on system conditions.

FIG. 61

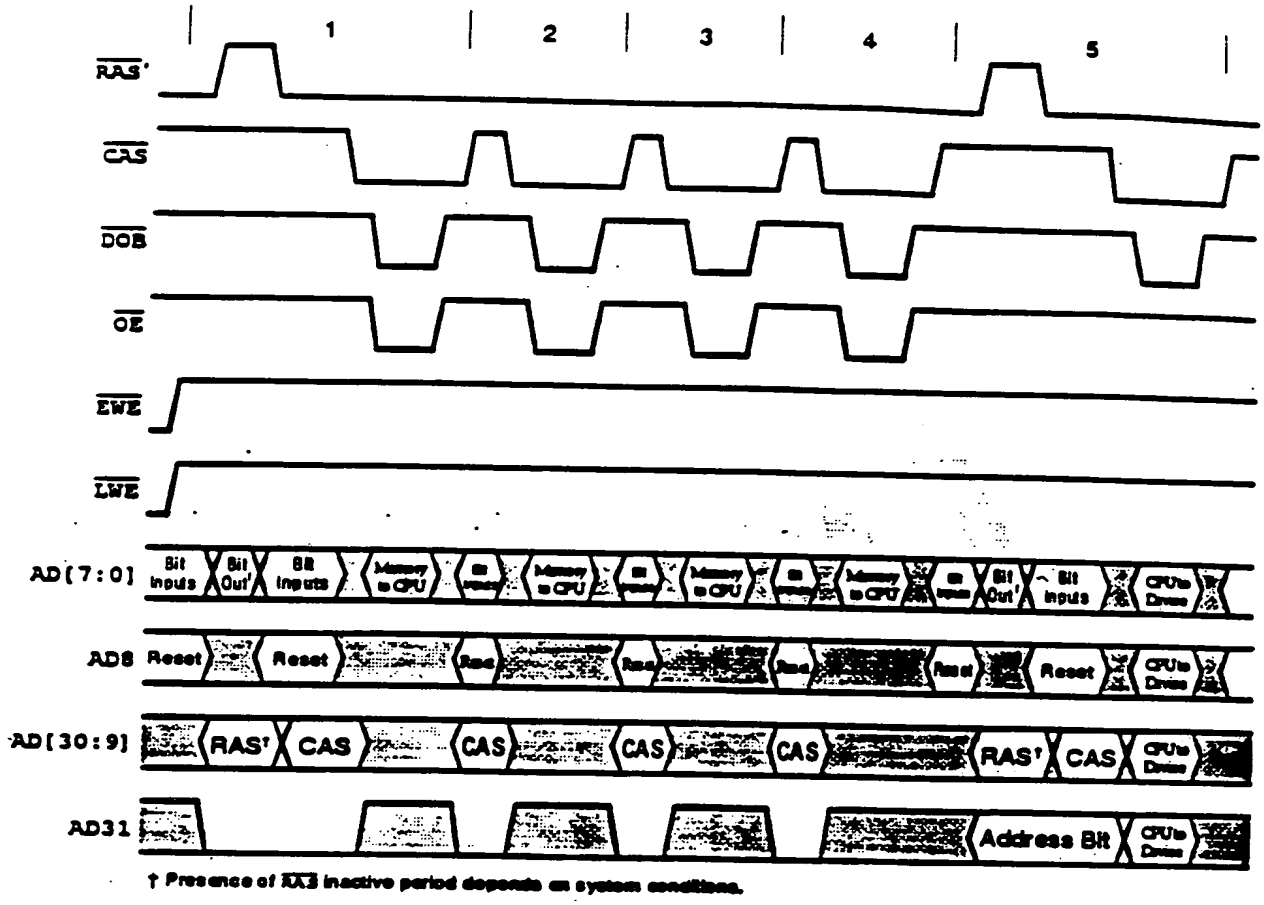

FIG. 62

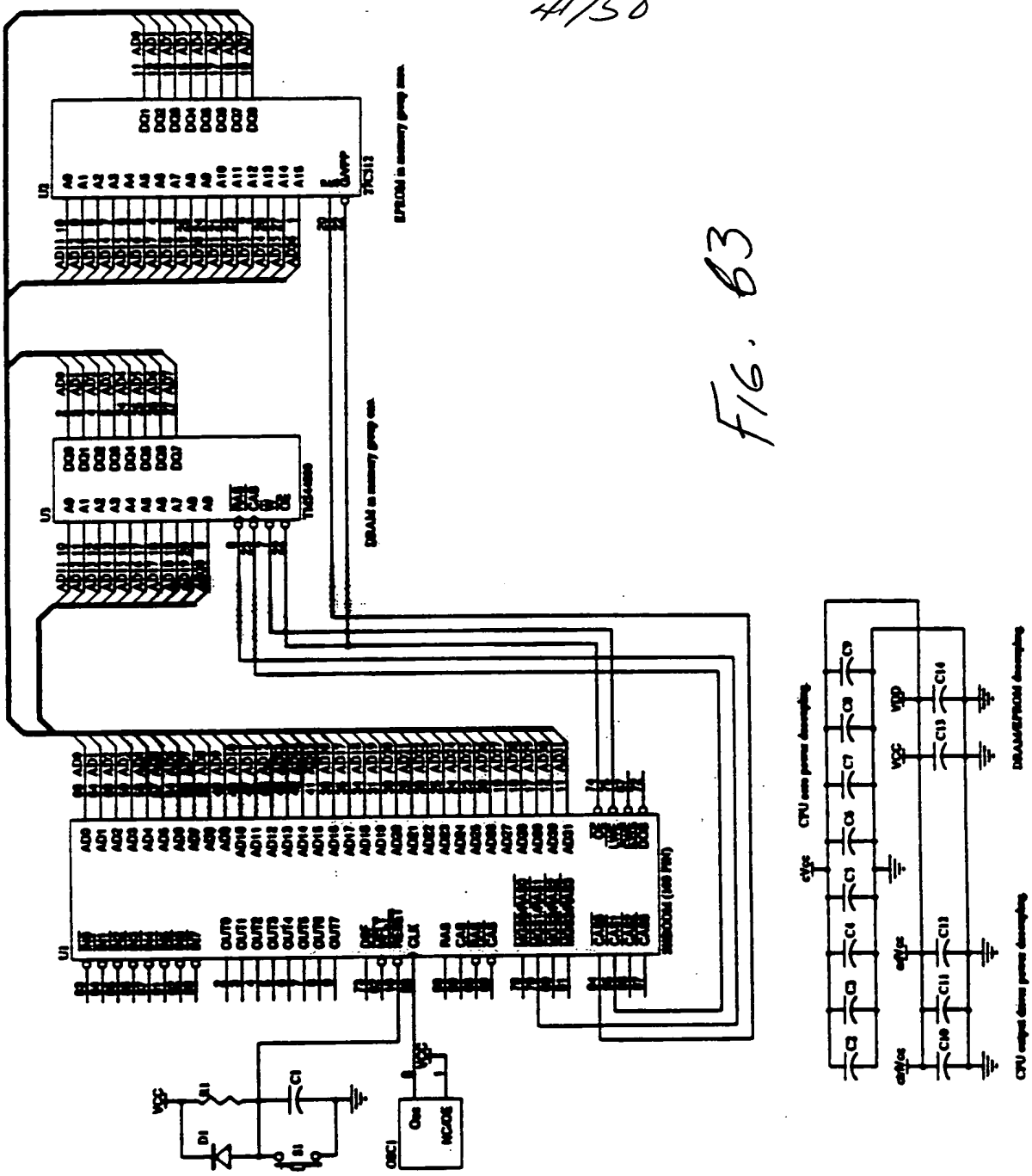

FIG. 63

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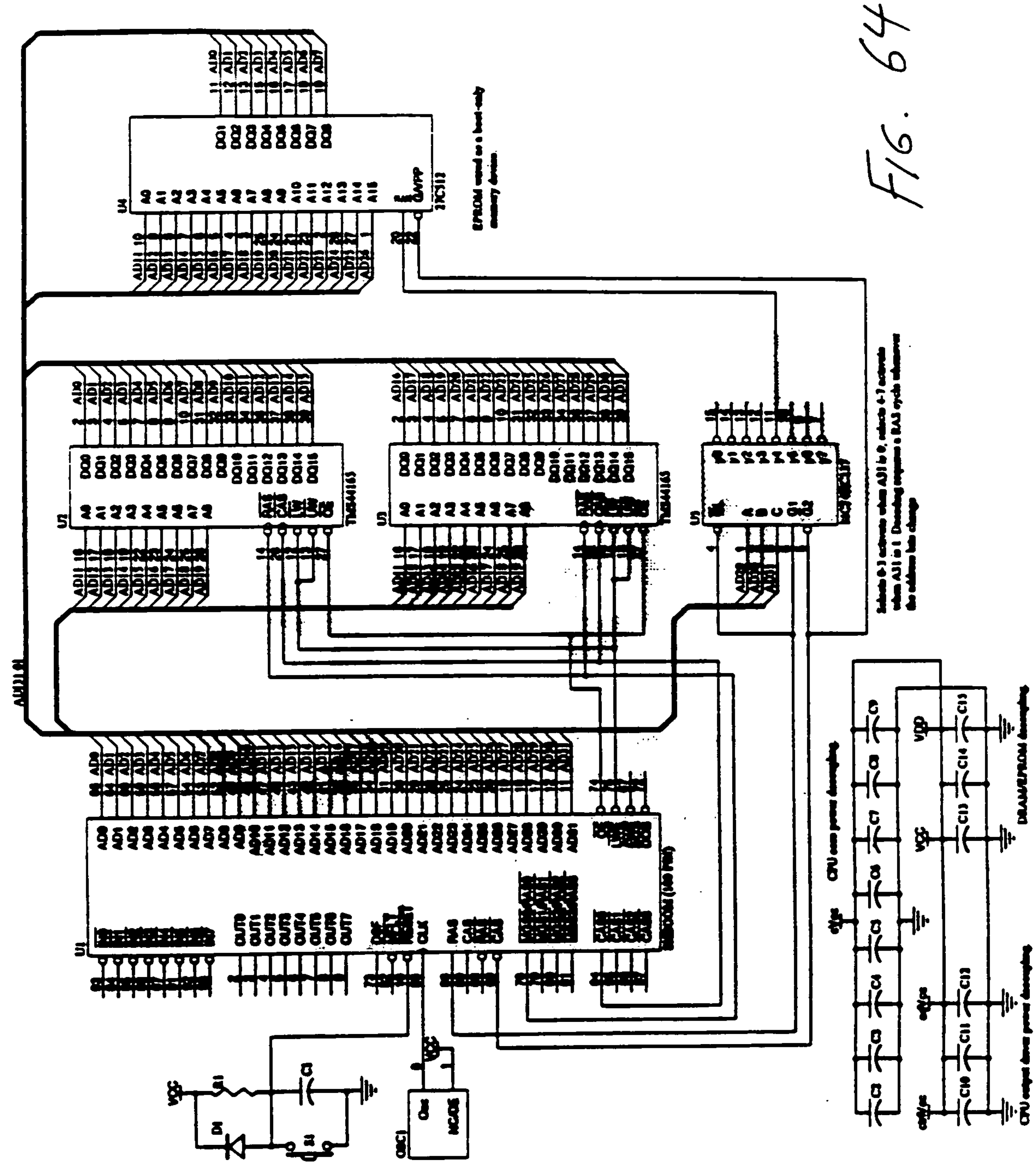

FIG. 64

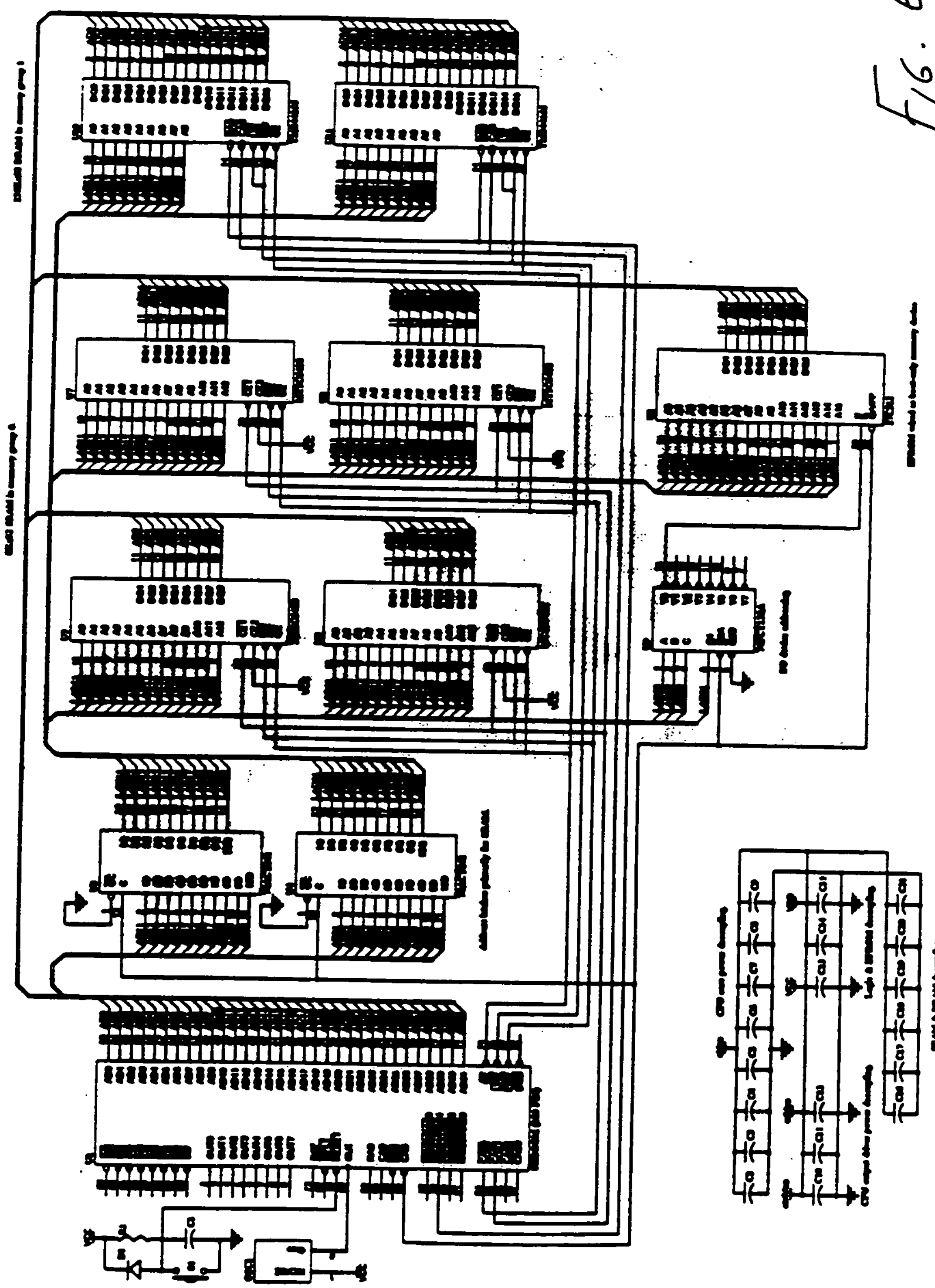

FIG. 65

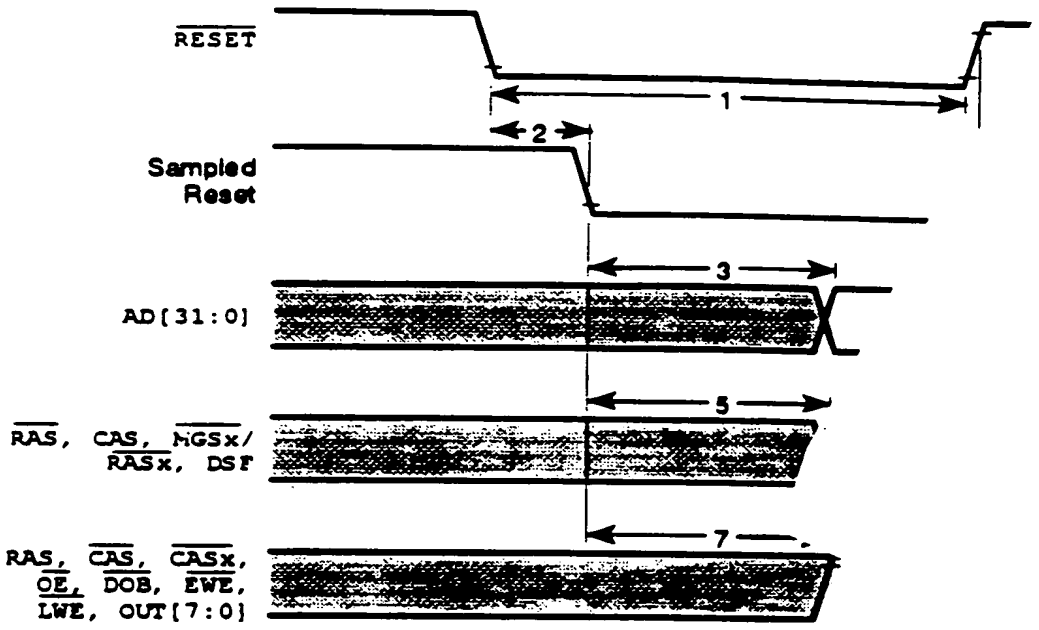

FIG. 66

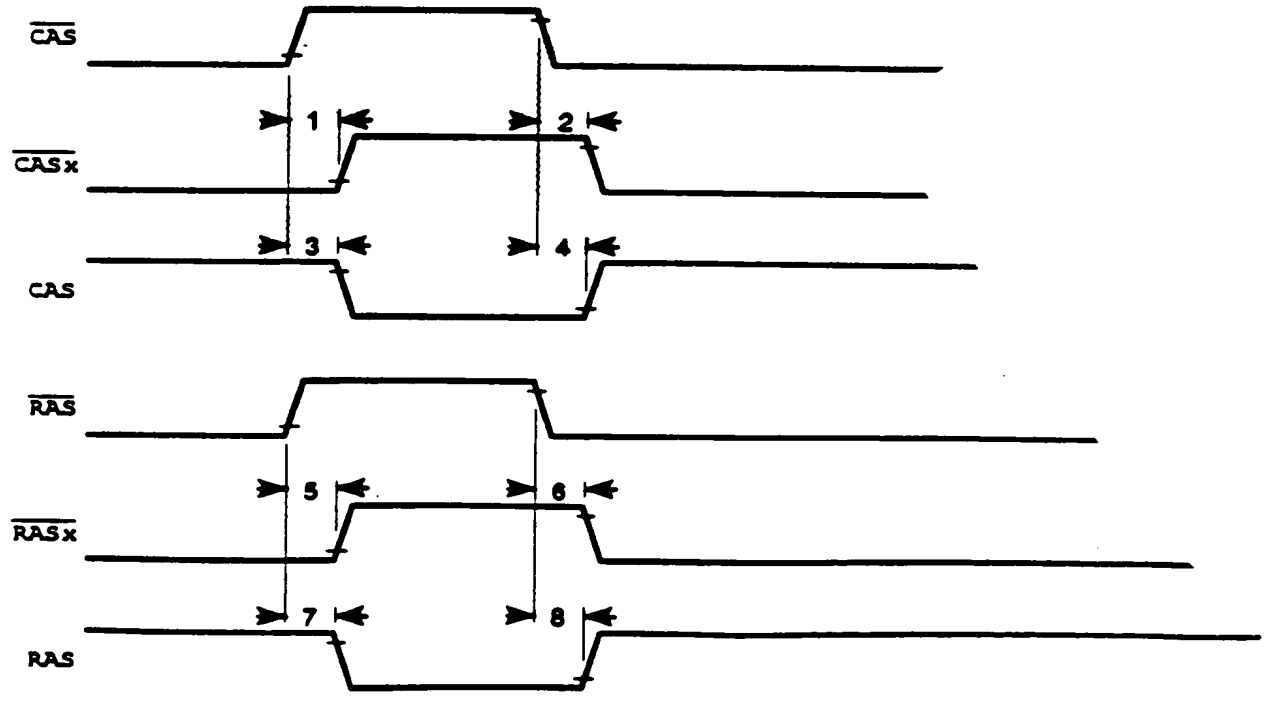

FIG. 69

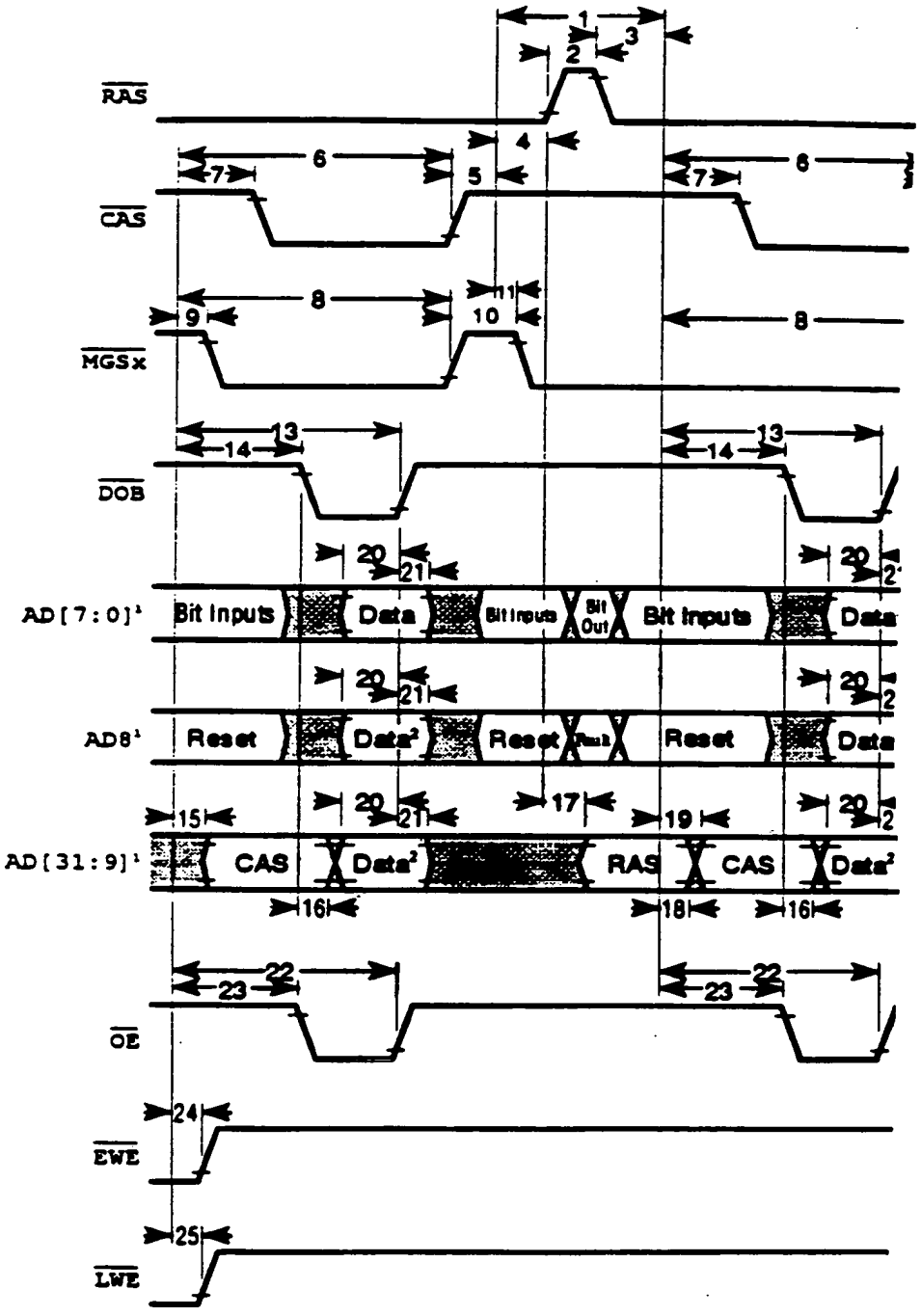

FIG. 67

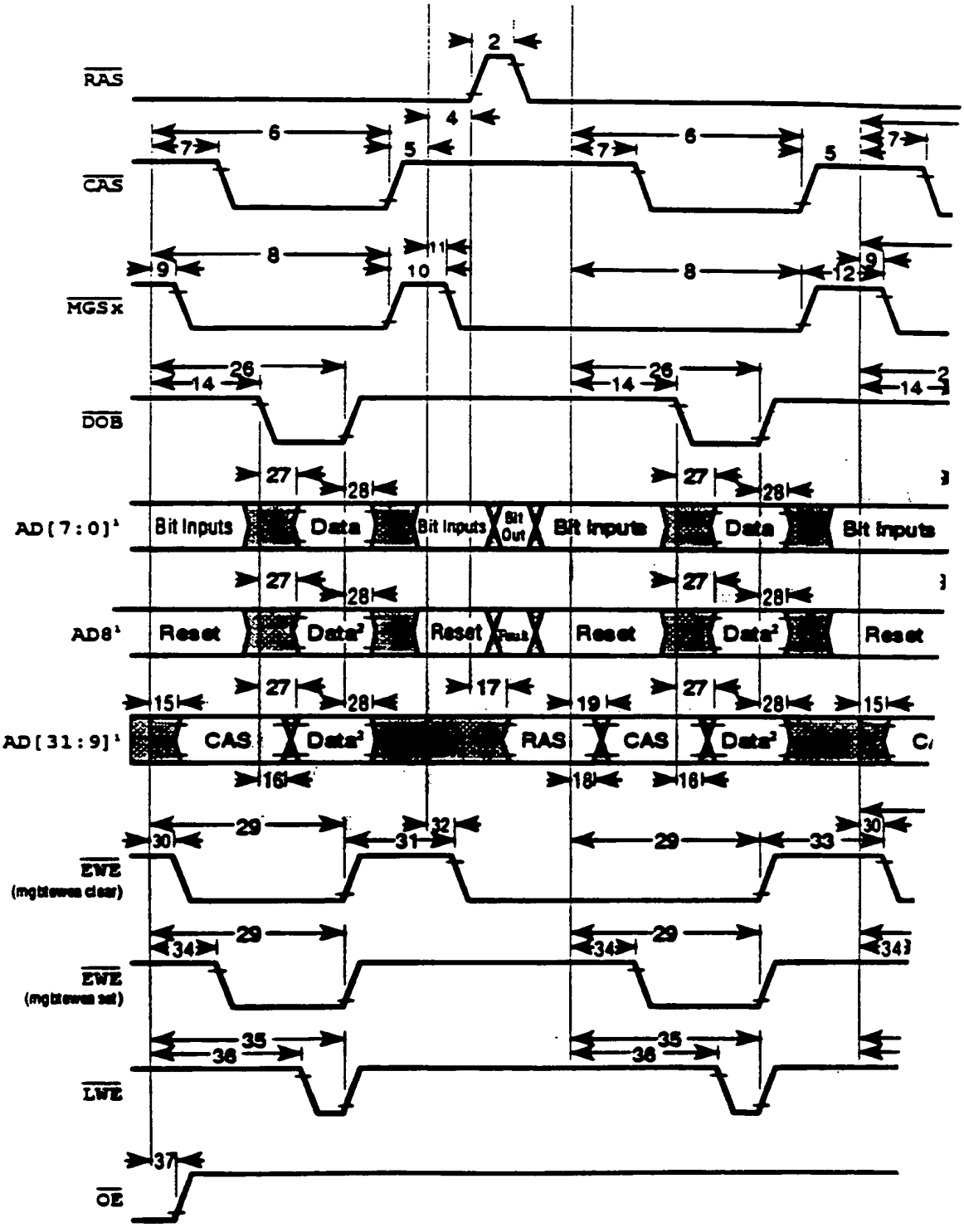
RAS
CAS
MGSx
DOB
AD[7:0]¹
AD8¹
AD[31:9]¹
EWE
(mgblewen clear)
EWE
(mgblewen set)
LWE
OE
Bit Inputs
Data
Bit Inputs
Bit Out
Bit Inputs
Data
Bit Inputs
Reset
Data²
Reset
Reset
Data²
Reset
CAS
Data²
RAS
CAS
Data²

FIG. 68

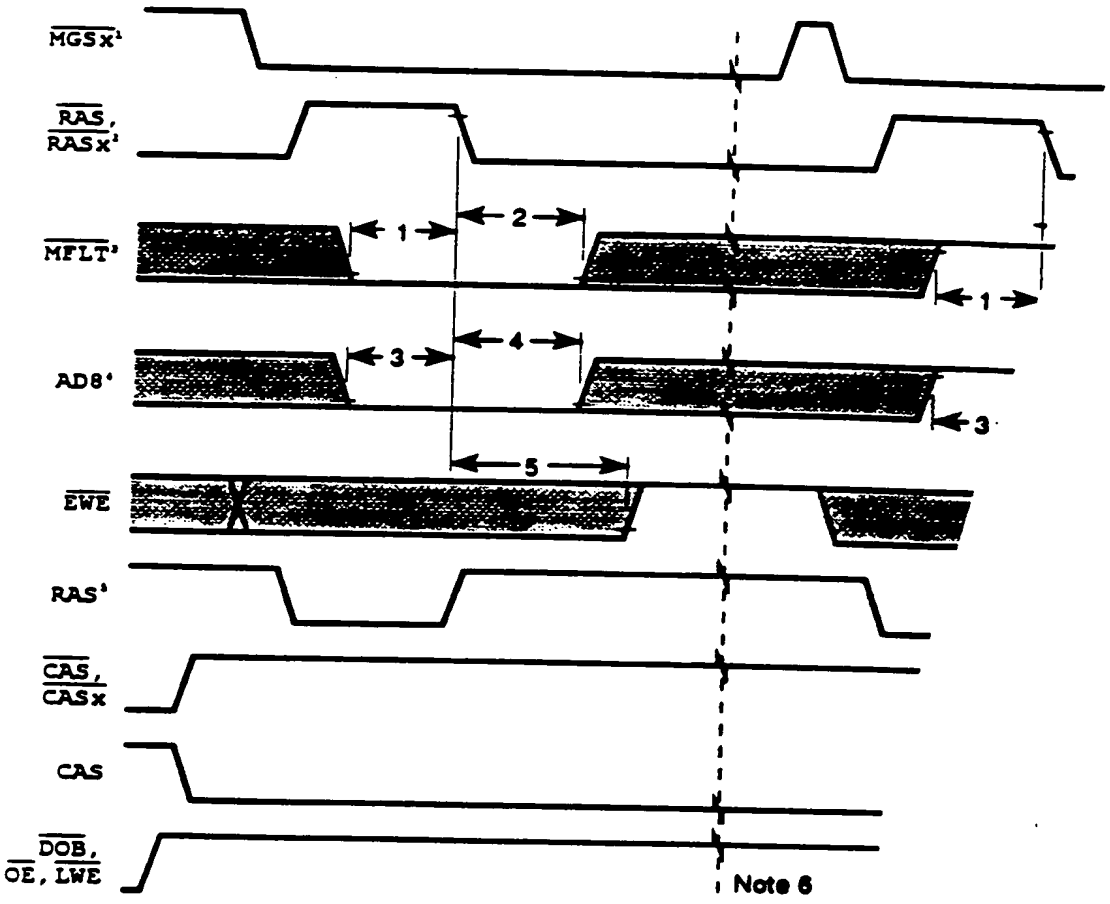

FIG. 70

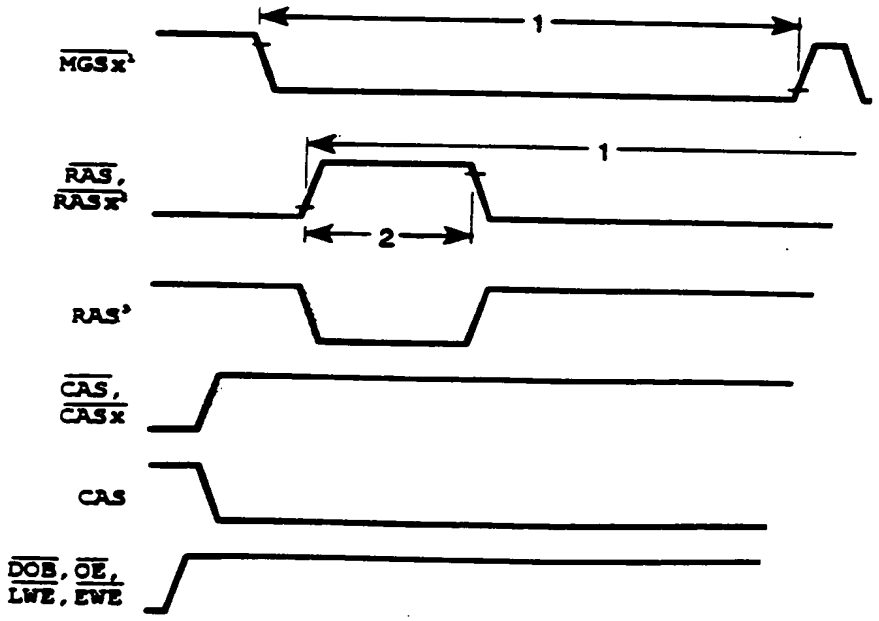

FIG. 71

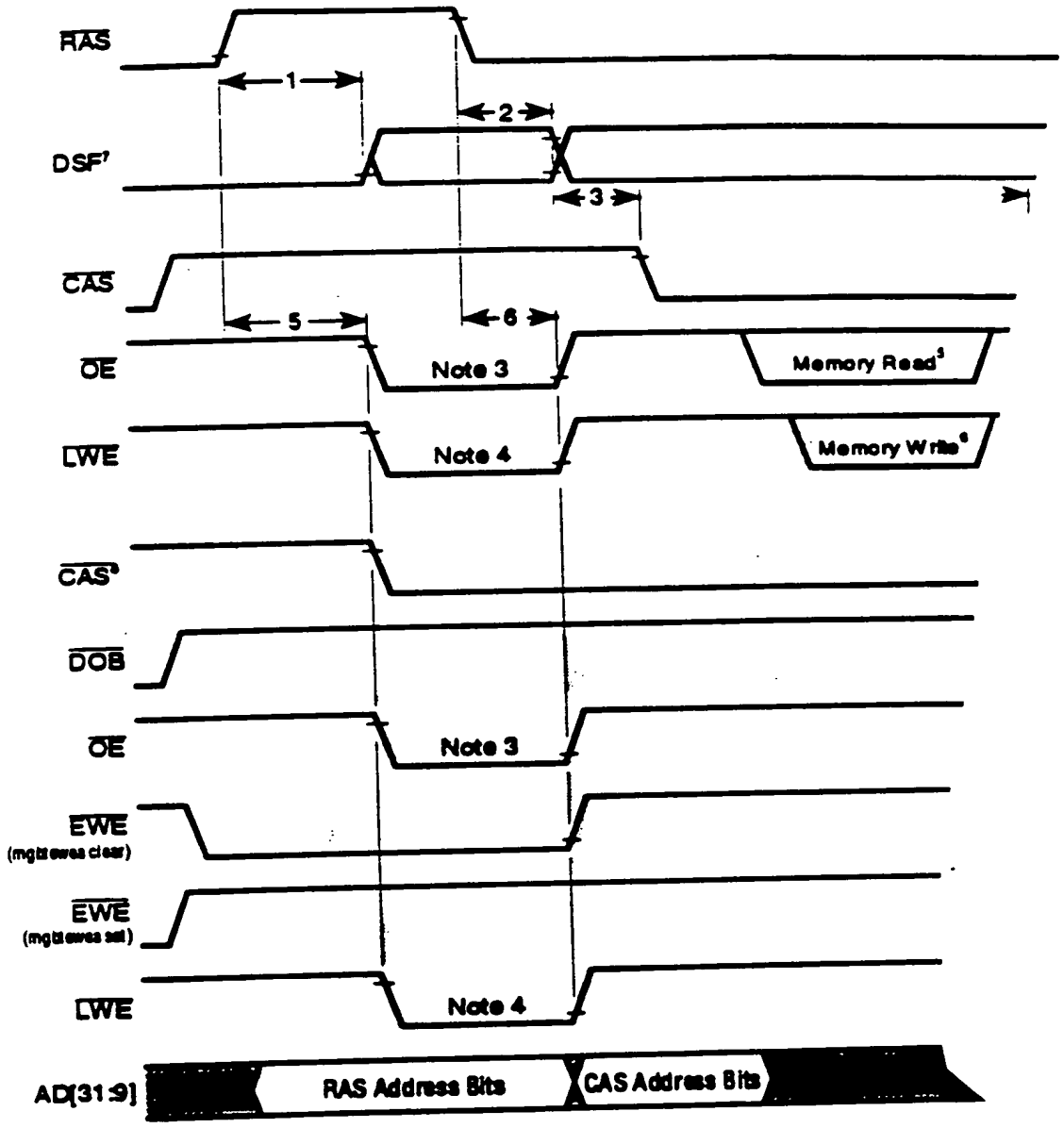

FIG. 72

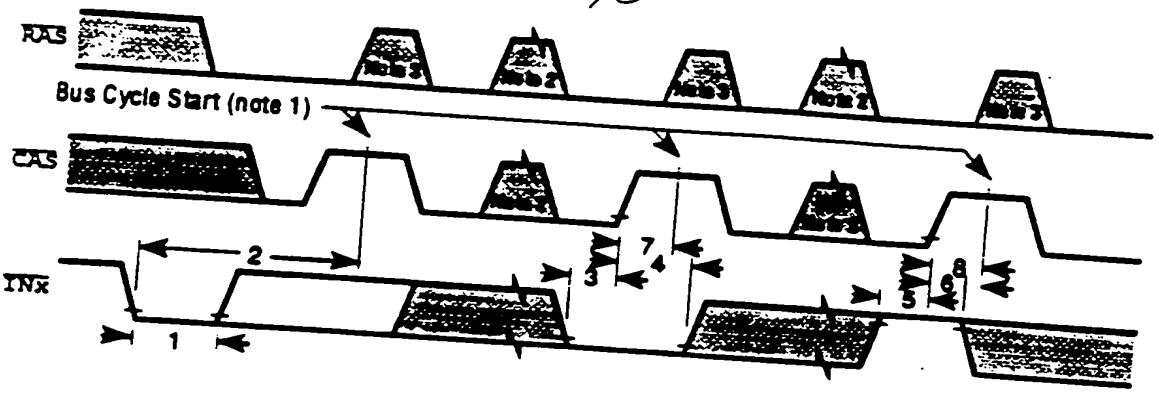

FIG. 73

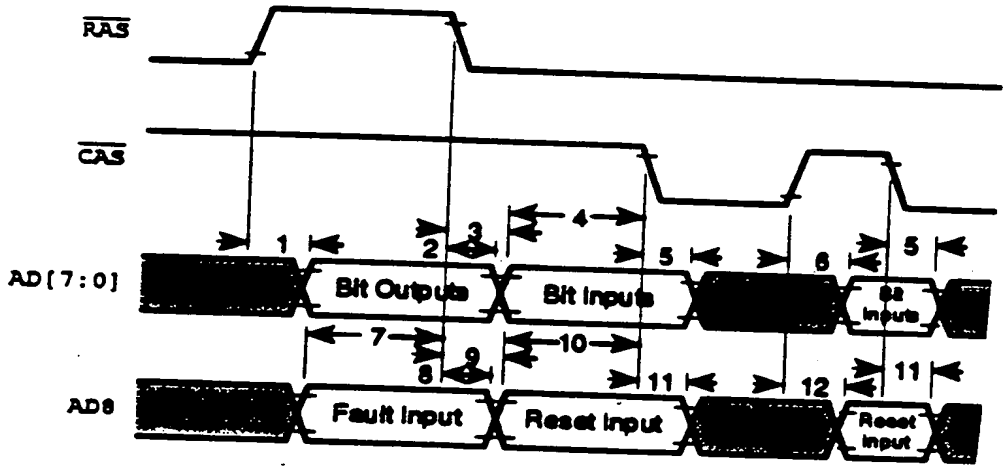

FIG. 74

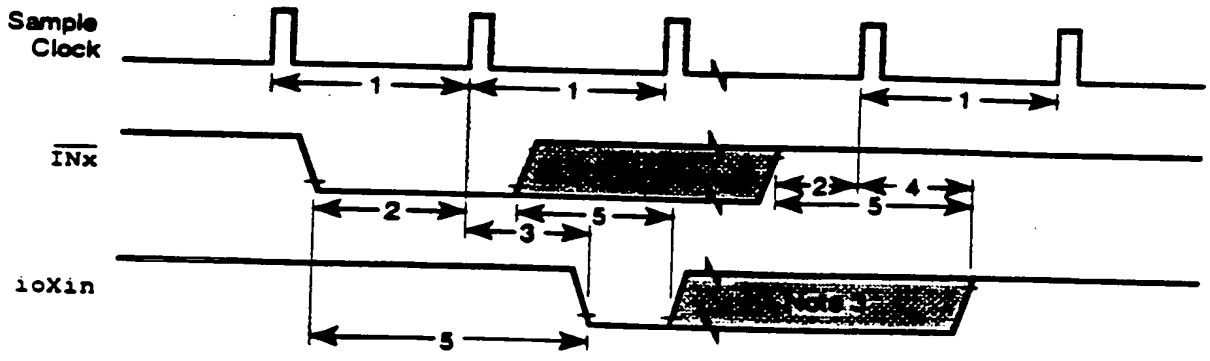

FIG. 75

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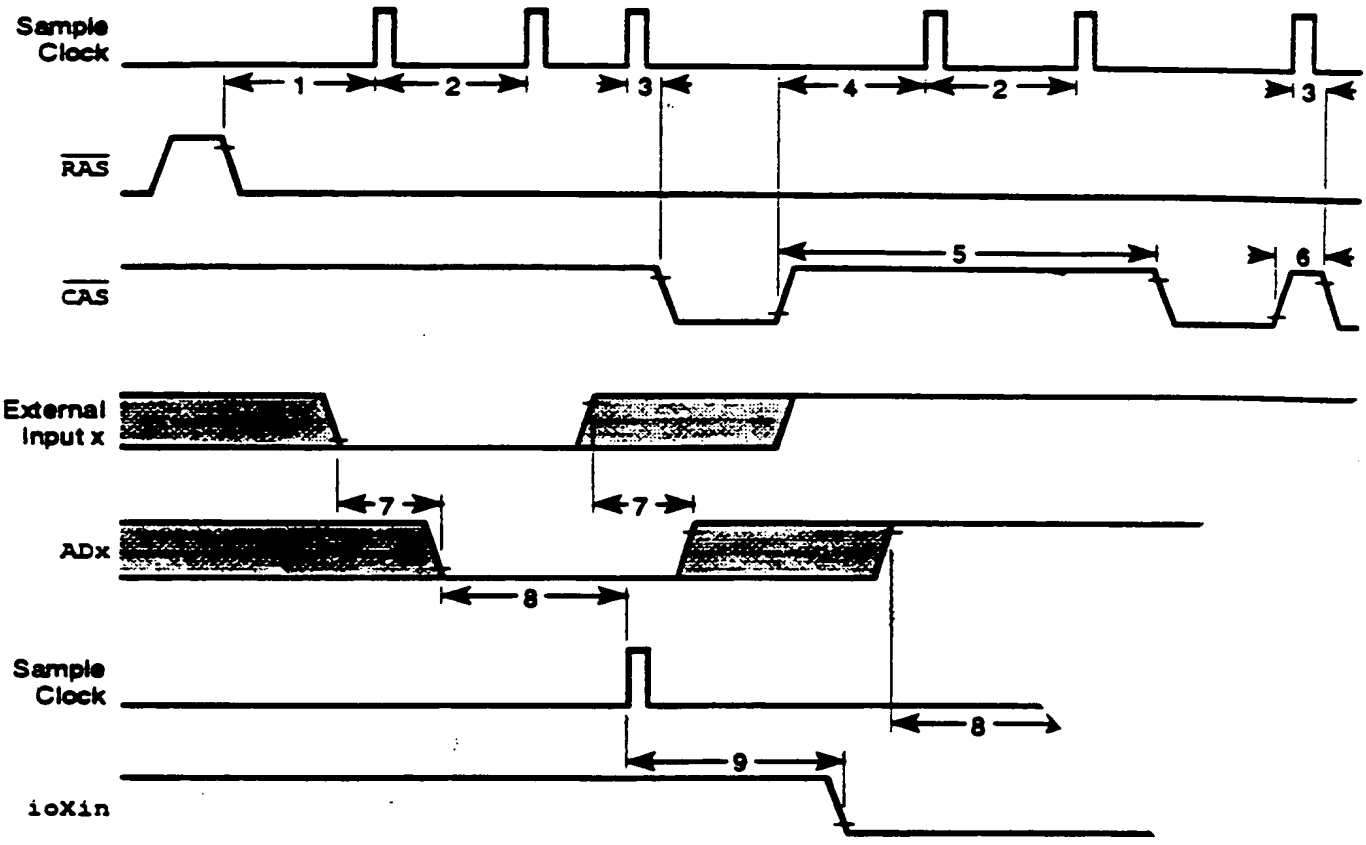

FIG. 76